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LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

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This report covers a program designed to realize the full potential of GaAs integrated circuits by expanding and improving fabrication and material techniques. The main accomplishment of the program was the successful implementation of the fabrication of integrated circuits on 3-inch diameter GaAs wafers. In addition, this program covered many activities related to GaAs IC processing. These include: work on semi-insulating material growth and characterization, investigation of ion implantation techniques (work carried out at the California Institute of Technology); evaluation of device uniformity, and investigation of its controlling factors; investigation of metallization yield and reliability, and improvements of processing techniques resulting from this study; design and testing of a multiplier and programmable shift registers/pattern generators; evaluation of mask programmable logic arrays to meet ERADCOMs needs for high performance communication systems; investigation of the hardness of GaAs ICs to total dose and transient ionizing radiation, and modelling of MESFET devices (this work carried out at North Carolina State University).

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FOREWORD

The research covered in this report was carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort was sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency and by the U.S. Army Electronic Research and Development Command. The contract was monitored by the Air Force Office of Scientific Research. The Rockwell program manager was Fred H. Eisen. The principal investigators for each organization were:

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Numerous other researchers were involved in the work reported herein. The principal contributors were:

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1.0 INTRODUCTION

This report covers a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. As suggested by the title, the main objective of this program was to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication and material techniques. The principal goal was to improve material and processing capabilities so that large wafers (over 3 inch diameter) could be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program was also directed toward an investigation of circuit reliability and the development of processing techniques capable of attaining the highest reliability. Circuit design advancements were also planned, as well as MESFET device modeling. The program also called for an investigation of radiation hardness of GaAs integrated circuits. In the last semester of the program, a feasibility analysis of mask programmable logic arrays for high performance communication systems meeting ERADCOM requirements was carried out. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. contributed to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

The highlight of the program was the successful implementation of the processing of 3 inch GaAs wafers, a capability which has not been emulated yet by any other domestic or foreign laboratory. Parametric data from the 3 inch wafers indicated significant improvement in process uniformity over the previous 1 inch process. The mask set used to launch the 3 inch wafer process contained 256 bit static RAMs, and the first successful operation of such a chip was demonstrated on the early lots of 3 inch wafers.

This report contains a discussion of many activities related to GaAs IC processing, material, circuit design, modeling, and radiation effects. Work at Crystal Specialties on growth of GaAs by the horizontal Bridgman method, as well as comparisons between Bridgman and liquid encapsu-

lated Czochralski (LEC) material are discussed in Section 2.0. The work done at the California Institute of Technology on dual implantations in GaAs and low temperature annealing of GaAs implanted layers is covered in Section 3.0. Section 4.0 contains the main topic of the program, IC processing. In addition to the development of the 3 inch wafer process, this section covers many other aspects of processing such as control of FET threshold voltages, variations to the standard process, metallization yield, fabrication of 1 inch wafers, and enhancements of circuit reliability from process improvements. Circuit design and test is covered in Section 5.0. In this section the design and test of a 8 × 8 bit parallel multiplier and of programmable shift registers/pattern generators are discussed, as well as a feasibility study of mask programmable logic arrays for applications which interest ERADCOM. Full details are presented in Appendix A. In Section 6.0 experiments to evaluate the radiation hardness of GaAs digital integrated circuits are presented. Both total dose and transient radiation sensitivity of the circuits are discussed. Finally, in Section 7.0, the work done at North Carolina State University on MESFET modeling is briefly summarized. More detailed information on this work can be found in Appendix B.

2.0 SEMI-INSULATING GaAs SUBSTRATE MATERIAL

Although the need for 3 inch diameter wafers makes the liquid encapsulated Czochralski (LEC) material the preferred one, the excellent quality of this material was not clearly established at the beginning of this program. Therefore, the growth of semi-insulating GaAs at Crystal Specialties by the horizontal Bridgman (HB) technique started on a previous program was continued.[1] This work is discussed in Section 2.1. Evaluation of HB material, and of LEC material grown at Rockwell or purchased from commercial suppliers is discussed in Section 2.2.

2.1 Growth of Semi-Insulating GaAs by the Horizontal Bridgman Method

Work at Crystal Specialties has resulted in the growth of several large area single crystals of GaAs using the horizontal Bridgman technique. (100) wafers cut from these crystals measured 2.5 in. wide and 4 in. long. The crystals were grown in a quartz boat 1 in. deep, 2.5 in. wide and 4 in. long. The seeds were oriented with the growth direction on the (110) axis so that the (100) axis is in the vertical direction. By cutting the crystal perpendicular to the vertical (100) axis, wafers as large as 2.5 × 4 in. could be produced. Since cutting equipment large enough to slice this large area was not available, the ingot was trimmed to about 2.5 × 3 in. before cutting.

Considerable progress has been made at Crystal Specialties in the reduction of dislocations generated during crystal growth by the horizontal Bridgman method. Single crystals with dislocation densities as low as 200 etch pits/cm^2 have been grown.

The crystals were grown in the (111) and (110) directions. The low dislocations were obtained by close control of the thermal gradients and arsenic pressure. Previously, the dislocation density of an ingot progressively increased toward the tail of the ingot. Using these new techniques of growth, the dislocations are considerably lower at the tail of the ingot. Typically, ingots have dislocations which vary from about 5×10^3 pits/cm^2 at

the front of the ingot to about 1×10^4 pits/cm^3 at the tail. The new ingots start at about 1×10^3 pits/ cm^2 on the front of the ingot, and improve to a value of about 200 pits/cm^2 at the back end of the ingot.

It is evident from this work that very low dislocation density material can be grown on a routine basis. Since twins and lineage arise from dislocations, it appears that lowering dislocation densities may allow for longer boats to be used without incurring in twinning and lineage problems. This may lead to improvements in yield and lower cost of production.

2.2 Evaluation of HB and LEC Substrate Material

During the early phase of the program, when processing was done on 1-in. square wafers, integrated circuit fabrication was carried out with LEC material on an experimental basis, while Bridgman-grown Cr-doped GaAs ingots were providing a major fraction of the substrates processed. In order to insure proper results in the IC fabrication process, qualification, testing and preselection of ingots continued to be required. The selection was based on (a) absence of thermal conversion during Si_3N_4 capped anneals, and (b) proper carrier density profiles obtained from representative Se implants. Of the 7 ingots grown by Crystal Specialties during the early phase of the program, 57% tested. Of these, 4 proved to be qualified for ion-implantation in approximate agreement with the previously observed long term yield.[1]

A portion of the semi-insulating ingots grown by Crystal Specialties were supplied as rectangular slices with dimensions approximately 1.5 × 2 in. grown in boats with square cross-section (rather than the customary semi-cylindrical cross-section). This technique, pioneered by Crystal Specialties, represents a significant advance towards the development of GaAs slices of large dimensions and standard shape (rectangular rather than round) as well as standard size obtainable using boat growth techniques.

The uniformity of substrate characteristics for the rectangular slice is an important question. It had previously been determined that the uniformity of threshold voltage obtained from the Rockwell implantation process is

influenced by the particular substrate used.[1] The substrate characteristics are nonuniform principally because of spatial variations in the concentration of Cr and residual impurities due to segregation effects during crystal growth. The square wafers were tested for threshold voltage uniformity and compared with the D shaped wafers. The results indicate that the uniformity is different, but appears to be strongly ingot dependent.

The substrate uniformity may be gauged by the standard deviation σ_T of threshold voltage among the test FETs fabricated on typical wafers. These test FETs are part of the process monitor test areas included on all mask sets, and are tested automatically for each wafer processed. The standard deviations obtained correspond to the variations in doping encountered for the Se implanted channel layer, over 24.5 × 24.5 mm square wafers. Measured values of σ_V are shown in Table 2.2-1 for both a highly uniform square ingot (ingot A) as well as for a square ingot of poor uniformity (ingot B). Values obtained for a representative D shaped ingot are shown for comparison. These results indicate that (a) the uniformity of threshold voltage is more strongly dominated by the substrate than the process, (b) the degree of uniformity achievable can be very high; (c) the results are ingot dependent in a way that is not currently understood. The pattern corresponding to the variations in threshold voltage is readily apparent in Fig. 2.1-1, which illustrates the depletion voltages measured by the C-V technique on a highly nonuniform wafer implanted with Se. A uniform gradient of depletion voltage is observed. The magnitude of the gradient observed correlates very well with the measured standard deviation of FET threshold voltage on processed wafers.

Table 2.2-1

Standard Deviations of Threshold Voltages Measured Across Processed Wafers from Representative Bridgman Ingots

Ingot		Shape	Quality	Standard Deviations (mV)
(A)	E122	Square	Uniform	45, 62, 60, 63, 64, 130
(B)	XS4570	Square	Non-uniform	165, 118, 151, 231, 320, 121, 149
(C)	XS4572	D	Typical	86, 52, 103, 80, 126, 180, 200, 154, 203, 73, 93

As efforts at Rockwell in the growth of GaAs ingots by the Liquid Encapsulated Czochralski (LEC) technique (conducted under IR&D funding) began to yield results, a number of integrated circuit lots of 1 inch wafers were processed with LEC material. DC characterization of test circuits on the process monitor areas distributed across the wafers was used to confirm that the LEC substrates exhibited excellent uniformity. Table 2.2-2 illustrates the average values and standard deviations of FET threshold voltages obtained for the wafers of three early lots fabricated on LEC material. The standard deviations - as low as 41 mV - are among the lowest ever observed. These results have been obtained both for ingots that were Cr doped and ingots that were grown undoped. In both cases the test FETs displayed a proper value of saturation current, in keeping with results observed using Bridgman-grown Cr-doped substrates.

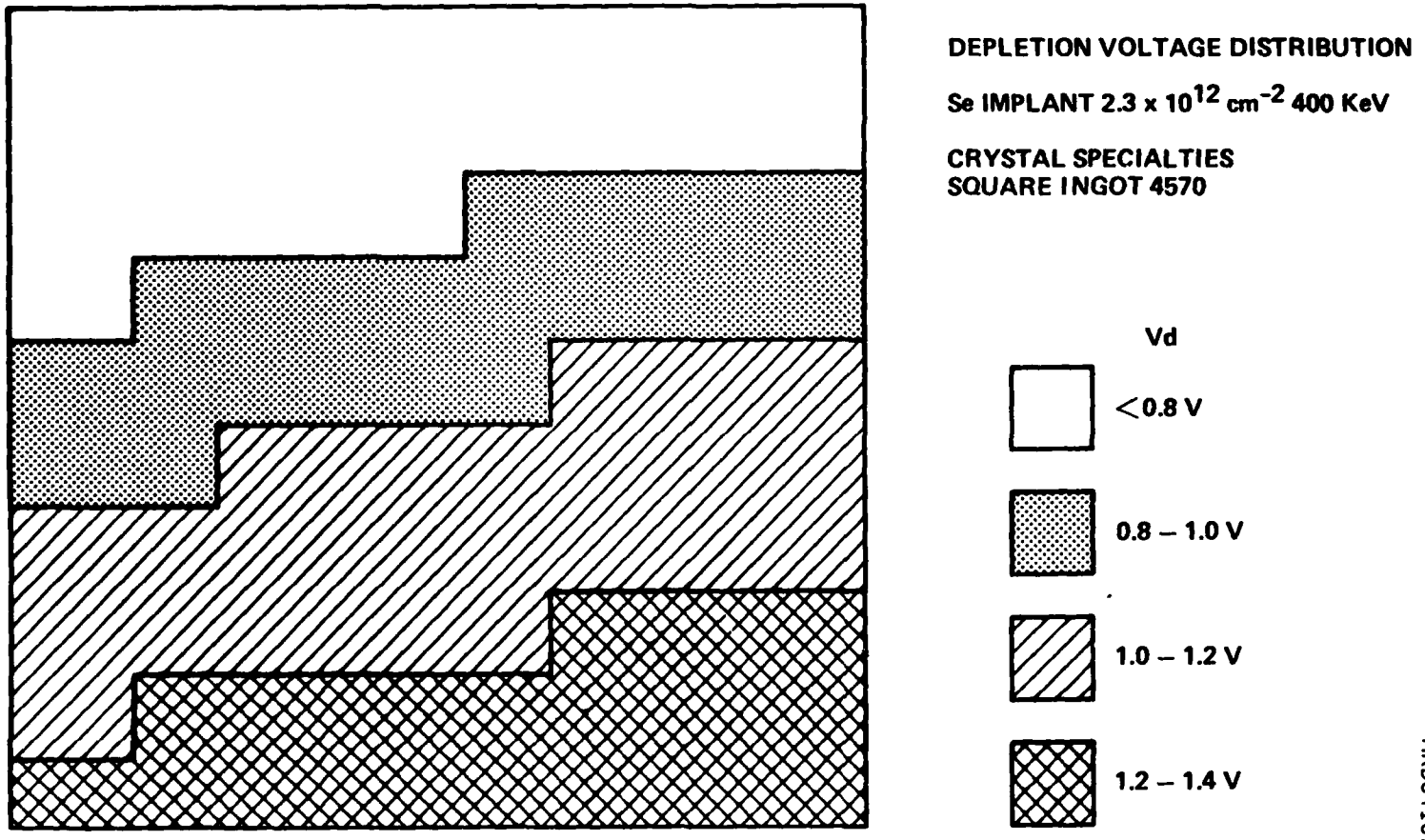

Fig. 2.2-1 Measured distribution of depletion voltage over a Se implanted wafer obtained from a Crystal Specialties square ingot exhibiting poor uniformity. The sample dimensions are 1 x 1 inch.

Table 2.2-2

Mean and Standard Deviation of FET Threshold Voltage Measured on Wafers Processed with LEC Substrates

Lot	Ingot	$\bar{V}$ (V)	σ_V (mV)
AR4-8	R4 (Cr doped)	1.08	48
		1.12	69
		0.99	56
		1.18	73
AR5-6	R5 (Cr doped)	0.99	62
		1.26	41
		1.18	64
AR5-8	R2 (undoped)	1.04	66
		1.18	47
		1.13	42
		0.85	41

The carrier density obtained with low dose Se implants was higher in the Bridgman grown substrates than in the LEC substrates. As a consequence, it is typically necessary to use a slightly higher implant dose in order to achieve a desired value of threshold voltage with the LEC substrates. It is of interest to determine the reason for this difference. One possible explanation is that a smaller fraction of the implanted donors may be electrically active in the LEC substrates. This hypothesis is effectively ruled out, however, by the data shown in Fig. 2.2-2, where the depletion voltage V_d that resulted for a series of Se implants is plotted vs implant dose for two LEC ingots and a representative Bridgman ingot. The values of V_d scale linearly with dose, with the same slope ($\sim$ 1 V/10^{12} cm^{-2}) for all the materials. This is the result expected for comparable activation of the Se in all the substrates. The offset in V_d is produced by a constant (dose independent) component of $N_{dr} - N_{ar}$ (where N_{dr} and N_{ar} are residual donor and acceptor concentrations) which differs among the substrates. The presence of a component N_{dr} due to residual Si in the Bridgman grown ingots has been previously discussed.[1] There may also be a slight net acceptor component N_{ar} in the LEC material, although further work is needed for its characterization.

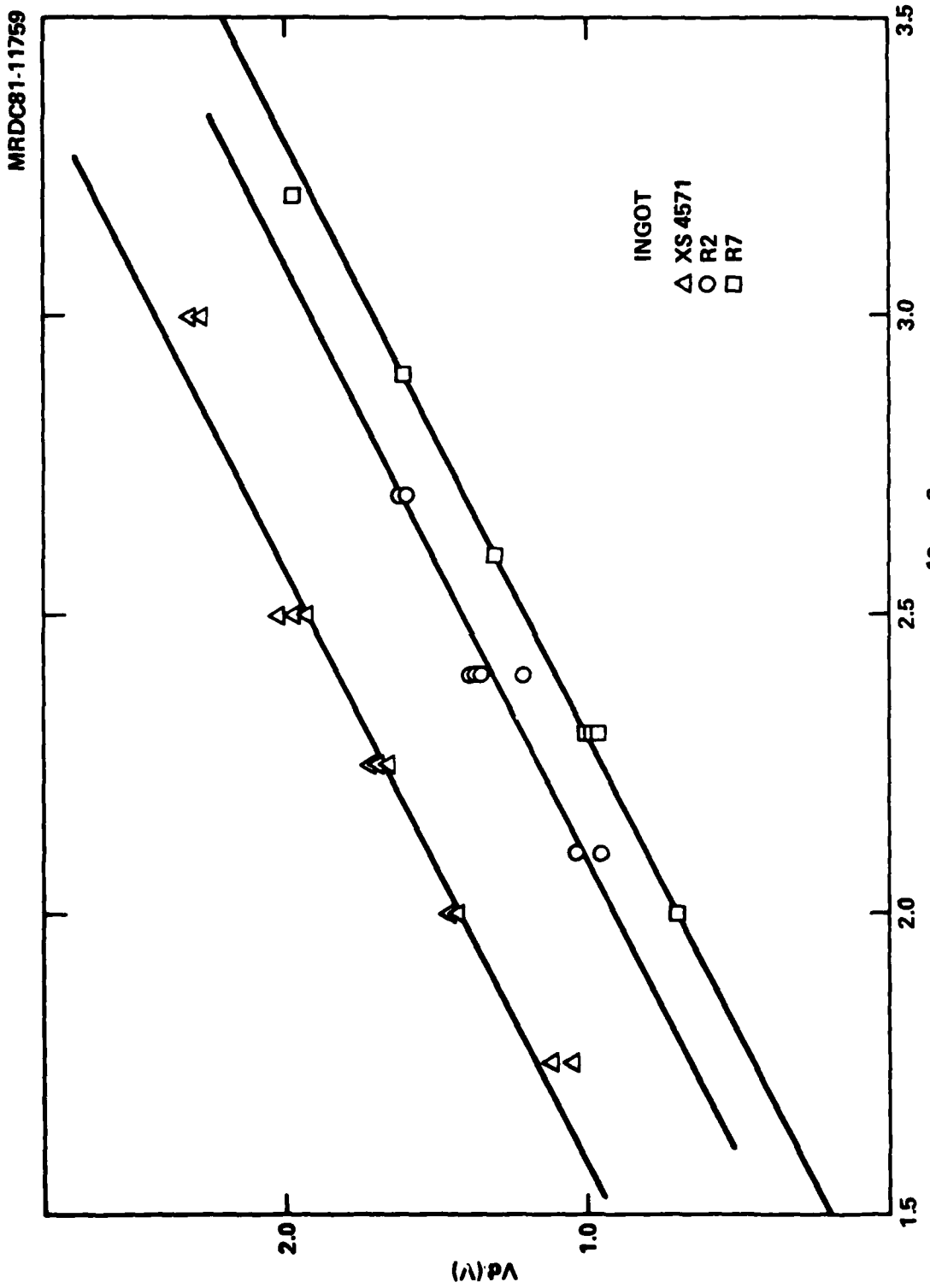

Fig. 2.2-2 Measured depletion voltage as a function of Se implant fluence for several substrates. The data indicate constant Se activation, but variable contributions of residual donors or compensating centers for the substrates.

The uniformity of LEC grown ingots along their length is also a topic of great interest. A measurement of the depletion voltage of Se implanted layers along the length of an LEC ingot was carried out and the results showed excellent uniformity. For this study, test chips were cleaved from sample wafers selected along the length of an ingot, and subsequently capped, implanted with Se and annealed together in the standard fashion. The depletion voltages, V_d, obtained for these test chips from C-V measurements are illustrated in Fig. 2.2-3. The excellent longitudinal uniformity is apparent in the less than 100 mV variation from front to tail.

The ingot used in the uniformity test corresponds to a worst-case study. In fact, for nearly all Rockwell-grown ingots measured, the bulk resistivity is uniformly high ($> 10^8$ Ω/□) along the ingot length. On several ingots, however, p-conductivity developed towards the tail region. The ingot of Fig. 2.2-3 corresponds to such a case, as determined by resistivity measurements of unannealed test chips, whose results are also shown in the figure.

The fact that p-type conductivity occurs in unimplanted material while no doping change occurs in Se-implanted layers is well explained by a compensation model developed as part of Rockwell's IR&D effort. In the unimplanted material, the carrier density is determined by the balance between carbon acceptors (uniformly distributed along the ingot length) and EL2 deep donors, whose concentration decrease along the ingot length because the material became progressively enriched with Ga during crystal growth. In the implanted n-type material, however, the varying EL2 concentration has no effect since these deep donors are neutral; the electron density is determined by the balance beteen the (spatially uniform) Se donors and the (spatially uniform) carbon acceptors.

As the program evolved, and encouraged by the good results obtained from the LEC material, a full transition to LEC substrates was made, well in time for the beginning of the processing of 3 inch wafers for which there is no other alternative to LEC material. In addition to Rockwell, material

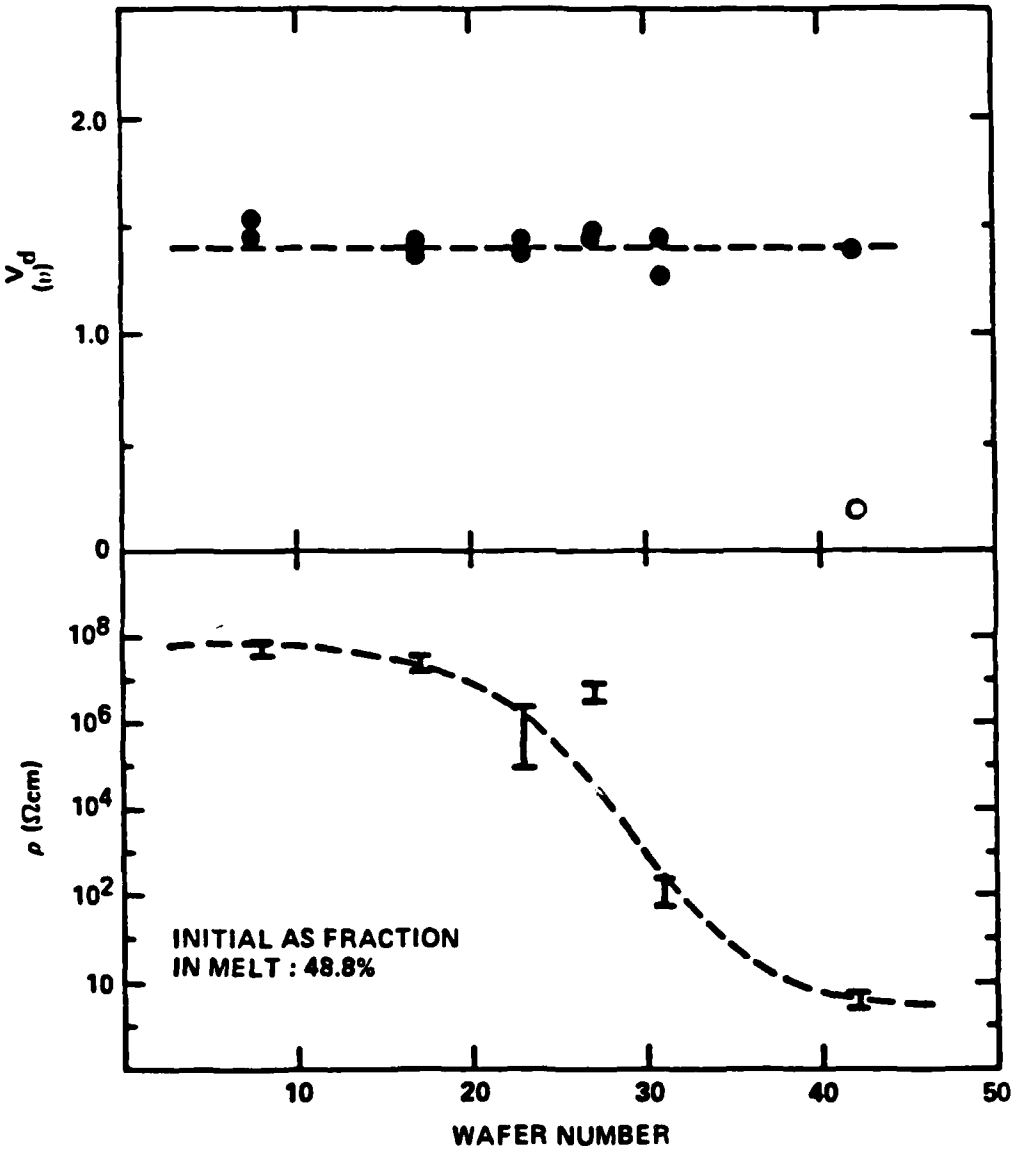

Fig. 2.2-3 Variation of the depletion voltage along the length of an LEC ingot. The data correspond to a worst case variation of bulk resistivity along the ingot, as shown by the lower curve.

suppliers of LEC material have been monitored. Qualification studies on commercial large diameter (3 inch) LEC GaAs materials produced by Cominco showed that most of their ingots are suitable for integrated circuit processing. Satisfactory resistivity after cap and anneal, and acceptable depletion voltages were observed in several qualified crystals.

Wafer preparation was also evaluated. The supplier (Cominco) was cooperative in realigning their flat system to provide for automatic crystallographic orientation of the large wafers coinciding with the flat orientation system developed in the Rockwell LEC growth program. Edge beveling was not yet available. Difficulties in polishing from the supplier still precluded the purchase of polished wafers. Therefore, all the materials were being bought as-cut for polishing at our facility. Figure 2.2-4 indicates the degree of flatness typical of purchased materials. The numerous fringes indicate a high center with several microns dropoff toward the edge. The Rockwell polishing capability results in as few as 3-5 fringes on the same size substrate. Upgrades in polishing equipment are under way at several commercial GaAs suppliers to improve their polishing results and significant improvements are, therefore, expected in the near future.

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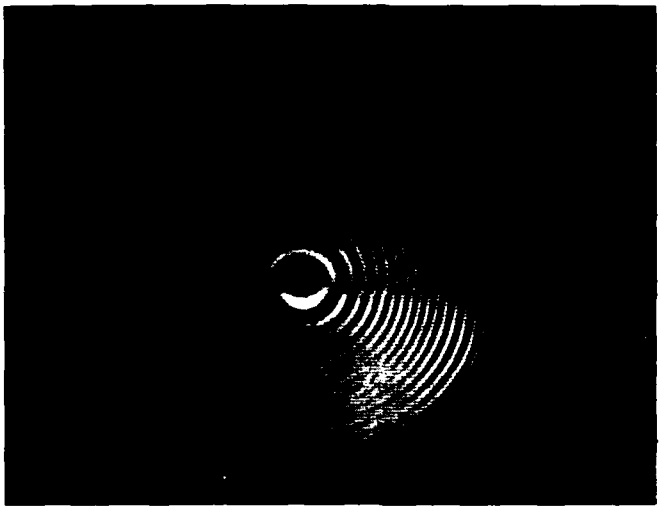


Fig. 2.2-4 Flatness photo of 3 inch polished GaAs wafer as received from the supplier. The wafer exhibits a high center.

3.0 ION IMPLANTATION IN GaAs

The activities at the California Institute of Technology were directed to the study of dual implantations of Si and As to determine whether it is possible to obtain high activation for heavy n-type doping, an objective that has eluded previous efforts. This work is discussed in Section 3.1. Efforts were also directed toward the investigation of low temperature annealing of implanted layers, which would provide many obvious advantages in integrated circuit processing. This work is described in Section 3.2.

3.1 Dual Implantation of Si and As

Room temperature implanted Si is an excellent n-type dopant in GaAs, generally producing a high degree of electrical activation for low-dose implants.[2] However, an upper 2×10^{18} cm^{-3} limit apparently exists on the achievable free electron concentration, attributed to the formation of neutral Si-Si pairs,[3] fixing the concentration for high-dose implantation. A series of experiments exploring the potential advantages of dual implantation with a complementary ion to enhance the Si electrical activation by maintaining local stoichiometric balance has been carried out in close cooperation with the Caltech group. These experiments have been completed and in summary, the results indicate that no increase in the upper limit of free carrier concentration was observed, though a given level of activation was achieved at reduced annealing temperatures.

Semi-insulating <100> Cr doped GaAs was implanted at room temperature with 150 keV Si to doses of 10^{13}, 10^{14} or 10^{15} ions/cm^2. Room temperature co-implantations of 360 keV As were also made to doses either five times less, equal to, or five times greater than the primary Si dose. The implanted samples were encapsulated with 2000 Å of reactively sputtered Si_3N_4 and annealed at 850 or 900°C for 30 min in flowing hydrogen. All implanted and annealed samples were characterized by sheet electrical measurements using a conventional van der Pauw method. A standard anodic stripping technique was employed for depth profiling of selected samples.[4]

The effect of coimplanted As on the free electron concentration and mobility profiles for samples implanted with 10^{14} Si cm^{-2} and annealed at 850°C is shown as an example in Fig. 3.1-1. LSS profiles for the Si and equal-dose As implantations are drawn for comparison. Arsenic has a pronounced effect on the free electron concentration. The limitation of the free electron concentration at $\sim 10^{18}$ cm^{-3} is evident in samples with little or no As. The difference in the two profiles should be considered insignificant and within experimental uncertainty. The integrated concentrations agree within 30% of the corresponding sheet values. An equal implantation of As at 10^{14} cm^{-2} reduces the free electron concentration near the surface by a factor of 25, and produces a large depth dependence. The mobility, in this case, shows the same inverse correlation with the free carrier concentration as is observed in bulk GaAs. With a large As dose, the free electron concentration reaches the saturation level though there is a step at approximately R_p of the LSS profile. The relative uncertainty of the points in the high As dose profile is less than 25% for the first 2400Å from the surface.

It is evident that enhanced Si substitutionality cannot be induced by altering the local stoichiometry with coimplanted As at room temperature. This result indicates that the threshold is not a function of compensating species, but rather an intrinsic property of Si in GaAs.

Silicon diffusion is not an important parameter in this investigation either. The profiles for single Si implantation extend to ~ 3.6 R_p for 10^{15} Si/cm^{-2} with 900°C annealing and to ~ 2.5 R_p for 10^{14} Si/cm^{-2} with 850°C annealing. It is evident from the profiles in Fig. 3.1-1 that As does not significantly influence Si redistribution.

The morphology of GaAs preceding annealing does not appear to be a factor restricting enhanced substitutionality. Extrapolation of results for the amorphization of GaAs by implanted Si, as established by Grimaldi et al using channeling,[5] indicate that GaAs is fully amorphous to a depth of ~ 2 R_p after room temperature implantation of 10^{15} Si/cm^{-2}. The subsequent As implantation into the amorphized layer is thought to merely extend the amorphous

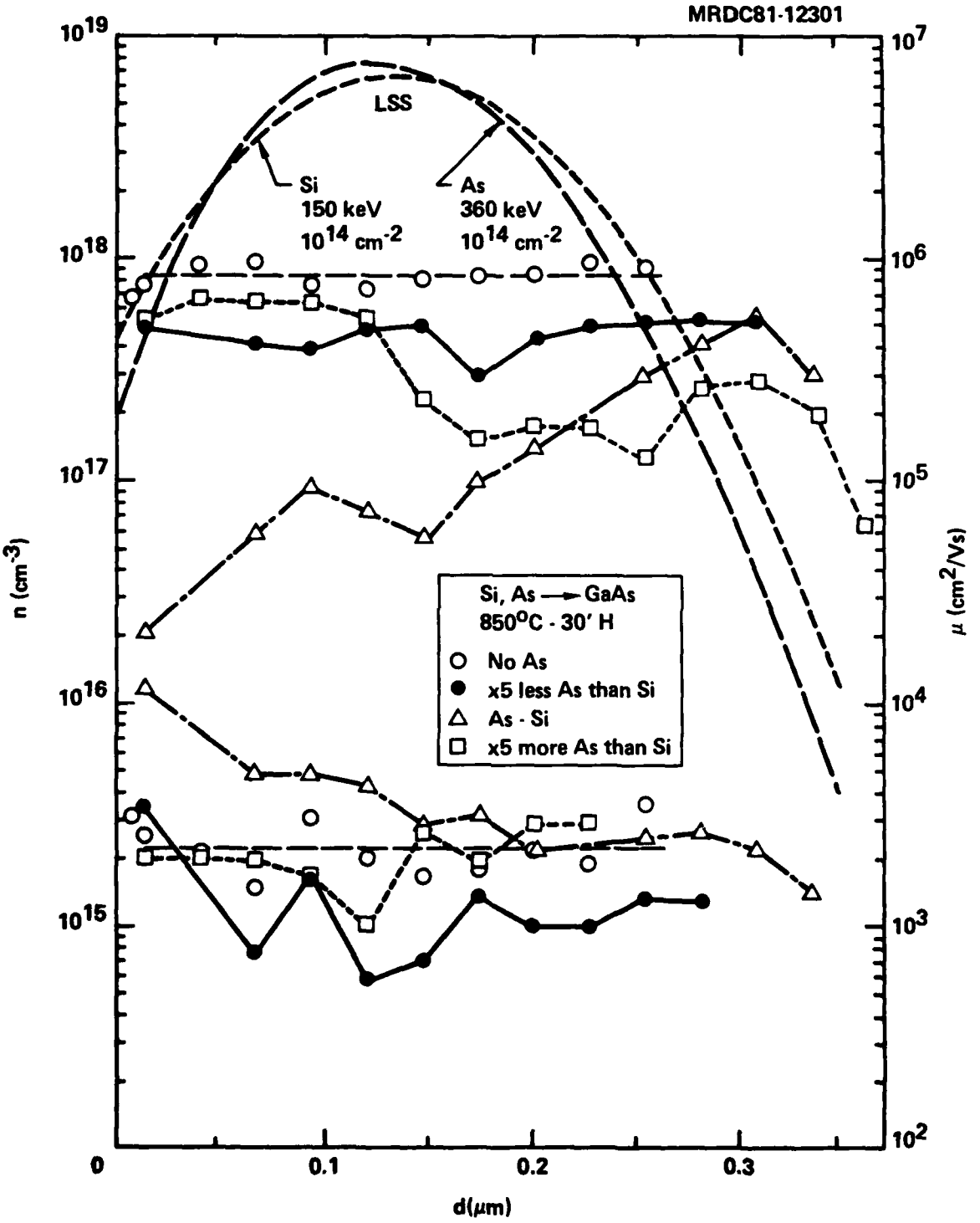


Fig. 3.1-1 Free carrier concentration and mobility profiles for GaAs.

region. In previous work it was shown for single specie implantation that regrowth is primarily governed by the initial amorphous thickness, irrespective of ion specie or dose. It therefore seems likely that the residual damage is qualitatively the same for all samples coimplanted with 10^{15} Si/cm^{-2}. Thus, regrowth of GaAs from the amorphous state is not a sufficient condition at high doses for As to enhance Si activation. In contrast, the implantation of 10^{13} cm^{-2} 150 keV Si leaves the GaAs polycrystalline. Extrapolation of results for the amorphization of GaAs by implanted As indicates that an amorphous layer may have been produced by implanting 10^{13} or 5 x 10^{13} cm^{-2} 360 keV As, though good regrowth is expected upon annealing because the amorphous layer would have had to be thin (< 500Å). There was certainly no amorphous layer after a 0.2 x 10^{13} 360 keV As implantation. It is therefore apparent that to maintain a crystalline structure is not a sufficient condition for enhanced activation with As either.

The electrical profiles for 10^{14} Si/cm^{-2} (Fig. 3.1-1) suggest that substrate morphology is a factor governing Si activation. In contrast to the behavior shown for 10^{13} and 10^{15} Si/cm^{-2}, coimplanted As has a strong influence on the Si activity at 10^{14} cm^{-2}. Note that this dose coincides with the transition region between the formation of a damaged single crystalline layer and the full amorphization of GaAs by room temperature implantation of Ar, As, S or Si in the energy range of hundreds of KeV. The As dose dependence observed in Fig. 3.1-1 most probably arises from an explicit dependence of the residual damage on the As dose in that transition region. The pronounced decrease in free electron concentration at the surface with 10^{14} As/cm^{-2} implantation is probably due to incomplete annealing. Sheet measurements (Fig. 3.1-1) show that the effect of As is less pronounced at 900°C than at 850°C. This further substantiates the conclusion that the effects seen in Fig. 3.1-1 are structural in origin. Since compensation by Cr gettering at the surface is not observed at other doses, Cr compensation is not a likely cause here either. Extrapolation of amorphization ranges reported for As in GaAs indicate that at 5 x 10^{14} cm^{-2} 360 keV As will produce a fully amporphous region extending to 1-2 R_p. The recovery of the free electron concentration observed

with 5 x 10^{14} cm^{-2} As implantation could therefore be attributed to regrowth from the amorphous state. Whatever the actual causes may be, it is evident that a rigorous characterization of the annealed layer in this transition region would require careful structural investigation of each particular case.

In conclusion, no indication has been found that Si substitutionality in GaAs can be enhanced by complementary dual implantations at room temperature. The 2 x 10^{18} cm^{-3} free electron limit for Si in GaAs does not appear to be associated with local stoichiometry or regrowth conditions. Coimplanted As does not have a perceptible effect on Si activation except in the transition region of ~ 10^{14} Si/cm^{-2}, where a complete annealing is delayed and a complex behavior is observed.

3.2 Low Temperature Annealing of Implanted Layers in GaAs

Room temperature implantation and low temperature ($\lesssim$ 600°C) regrowth have been subjects of investigation at Caltech and several other laboratories recently.[6-10] The main motivation for this work has been the hope of simplifying the process of electrical activation of ion implants into GaAs, and the wish to explore crystal regrowth properties in 3-5 compounds. In recent studies[6] it was shown that <100> GaAs that has been amorphized to a depth of $\lesssim$ 400Å by implantation can regrow at 400°C with a crystal quality that appears from spectra of channeled He backscattering to be almost as good as that of virgin material. More recently, the regrowth process for shallow implantations of dopant Te ions. has been explored. Te was chosen 1) because it is a well known n-type dopant in GaAs, and 2) because Te_2^+ molecules can readily be formed by ionization of Te vapor, facilitating low energy implantations. The question addressed was whether electrical activation could be achieved by low-temperature regrowth of shallow amorphized GaAs layers.

Semi-insulating <100> wafers of Cr-doped GaAs were implanted at room temperature with 80 keV Te_2^+ molecules to doses of 1 × 10^{14} and 2 × 10^{14} atoms cm^{-2}. According to the tabulations of Gibbons et al.,[11] 40 keV incident Te atoms should have a projected range in GaAs of 144Å, with a standard deviation

of 63Å. Annealing was conducted at 400°C in flowing dry argon for 60 min. Since the regrowth rate of <100> GaAs at this temperature is known to be at least 130Å min^{-1}, it is expected that all possible regrowth must have been completed in this time. Backscattering analysis was conducted with a 1.5 MeV incident He^{+} beam channeled along the <100> direction. A glancing exit geometry (scattering angle = 98°) was used to increase the depth resolution.

The spectra from the sample implanted to a dose of 1×10^{14} cm^{-2} are shwon in Fig. 3.2-1a, together with a spectrum for a channeled incident beam from an unimplanted GaAs sample. It is evident that the implantation created an amorphous layer with a thickness of ~ 500Å. One can also see that the annealing resulted in good regrowth of this layer back to the sample surface. The spectrum for channeling incidence deviates only slightly from that obtained with virgin material, viz. a slightly larger surface peak caused by greater surface disorder and slightly greater dechanneling. Similar spectra are shwon for the implantation to a dose of 2×10^{14} cm^{-2} in Fig. 3.2-1b. Here the initial amorphous thickness is ~ 600Å, and again the backscattering spectrum with the channeled beam indicates excellent regrowth, the beam sensing only a low concentration of added defects. For both implantation doses, the abundance of Te atoms was too low for the Te signal in the backscattering spectra to be discerned in a statistically significant manner.

Sheet resistance measurements were performed on the samples by the van der Pauw method both before and after furnace annealing. The results are shown in Table 3.2-1. The values are high after implantation, but increase even further as a result of the annealing. Such an increase of resistance has been observed previously for GaAs implanted with either donor or acceptor ions[12,13] and more recently by Kular et al.[7] The conductivity after implantation has been interpreted as a thermally assisted hopping process associated with localized states within the forbidden gap.[12] Low temperature annealing is believed to slightly order the material decreasing the number of localized states and increasing the room temperature resistivity.[7]

Table 3.2-1

Four-Point Probe Sheet Resistances
(Estimated Uncertainty ~ 10%)

Implantation Dose	R_s (MΩ/□) Implanted	Implanted & Annealed
1×10^{14} Te cm^{-2}	0.65	2.65
2×10^{14} Te cm^{-2}	0.50	2.50

The conclusion from this study is that although the lattice can apparently be reordered to a near virgin state by low temperature anneal, very little electrical activity of the implanted dopant is obtained.

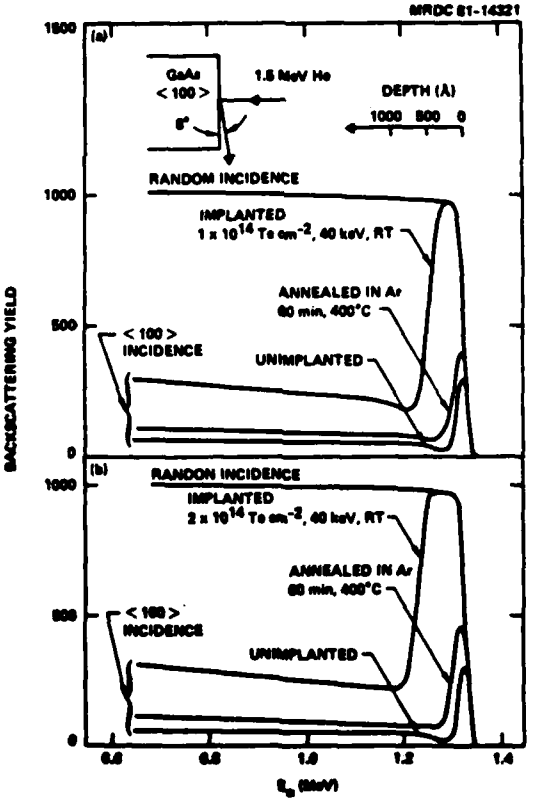


Fig. 3.2-1 Backscattering energy spectra of 1.5 MeV He^+ ions at random and <100> incidence. The sample was GaAs implanted at room temperature with 40 keV Te ions to doses of 1×10^{14} cm^{-2} (part a) and 2×10^{14} cm^{-2} (part b). Spectra are shown for the samples both before and after annealing in flowing Ar at 400°C for 60 min. Channeling spectra obtained with unimplanted GaAs are also shown for comparison.

4.0 INTEGRATED CIRCUIT PROCESS DEVELOPMENT

One of the main accomplishments of the program was the implementation of the processing of GaAs digital integrated circuits on 3 inch diameter GaAs wafers. This subject is discussed in Sections 4.6 and 4.7. Several other aspects of the process technology from control of FET threshold voltage to improvements in process leading to higher reliability are covered in sections, 4.1 through 4.5.

4.1 Reproducibility of FET Threshold Voltage

The control and reproducibility of the electrical characteristics of the FET channel implant are critical concerns for high yield fabrication of IC's. The channel (n^-) implant determines the threshold voltage for switching of the logic gates, and this voltage must be tightly controlled particularly for low voltage, low power IC's.

The technological development and investigation of the n^- implants has been an ongoing activity at Rockwell. Significant progress has been achieved, and for a statistically significant period of time, reproducibility has been satisfactory for high yield fabrication of high speed low power SDFL circuits. This result is evident in the data of Fig. 4.1-1, which show the distributions of threshold voltage obtained on all the 1 inch wafers processed throughout a period of over 6 months. The results were obtained by automated probing of 1 μm gate FETs distributed across the processed wafers. A histogram (Fig. 4.1-1) was made for the average threshold voltages obtained from each wafer. The overall average threshold voltage was 1.12 V (as desired for low-power, high speed depletion MESFET devices), while the standard deviation of V_T in Fig. 4.1-1 was 110 mV, well within the range required for SDFL circuits. The results include 55 consecutively processed wafers, corresponding to 14 lots and 8 different GaAs substrate ingots. Most of the wafers correspond to Bridgman grown substrates (5 ingots), although the Rockwell grown LEC substrate materials are also represeneted (3 ingots). Comparable control over

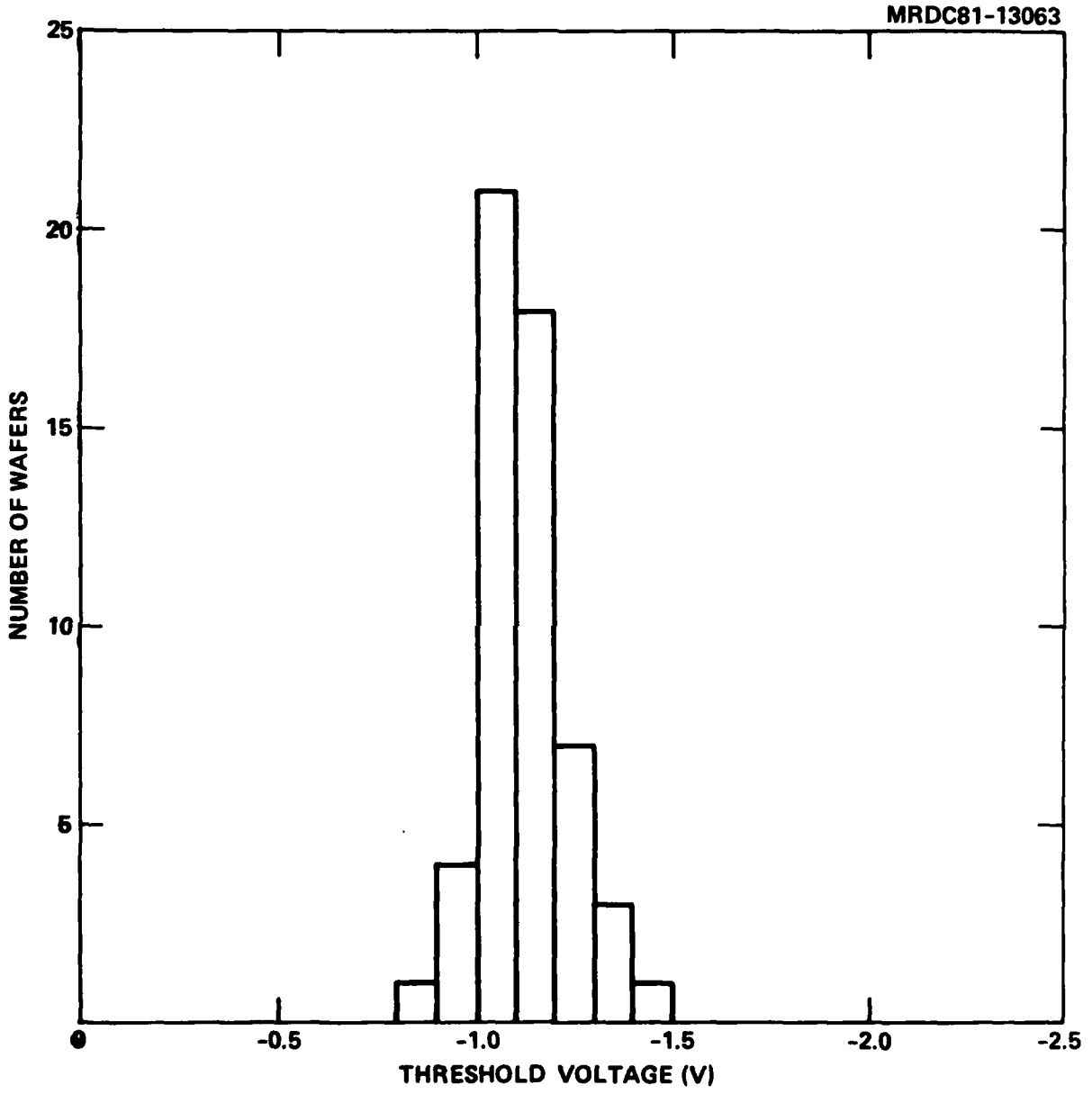


Fig. 4.1-1 Distribution of FET threshold voltage observed in 55 consecutively processed wafers over a 6 month period

V_T have been obtained for both types of substrates, provided ingot qualification tests are used for material selection, and implant fluences for IC wafer lots are chosen on the basis of test results with similar material. However, on the basis of a fixed implant dose, unselected ingot process, the LEC materials display significantly better reproducibility.

Data on uniformity of V_T across the wafers have similary been good over an extended time. For the same 6 month period, the median standard deviation of V_T across the 1 inch wafers has been only 64 mV. The uniformity of the LEC grown substrates has been significantly better (median standard deviation of V_T of 55 mV) than that for Bridgman substrates (median standard deviation of 84 mV). The superior unfiormity is expected on the basis of the improved purity of the LEC material, as well as its growth size and geometry which are better adapted to decrease the effects of impurity segregation during crystal growth.

A long-standing problem with the investigation of factors which influence the reproducibility of ion implanted layers has been the difficulty of distinguishing implant variations that are due to process differences, from implant variations due to differences between substrate material properties. Therefore, data have been accumulated to separate the individual contributions of these two effects.

In order to observe the magnitude of the process-related variations alone, a test chip from a fixed control ingot was included in each of 47 different implant runs carried out over a period of 9 months. The test chips were processed in a nominally identical way (with, for example, nominally identical Si_3N_4 encapsulant thickness and implant dose). Measurements of the depletion voltage V_d (voltage necessary to deplete the carrier density to 10^{16} cm^{-3}) yielded the results shown in Fig. 4.1-2. The standard deviation of V_d over this distribution was found to be 153 mV (after excluding 12% of the runs which yielded anomalously low activation, probably related to contamination effects).

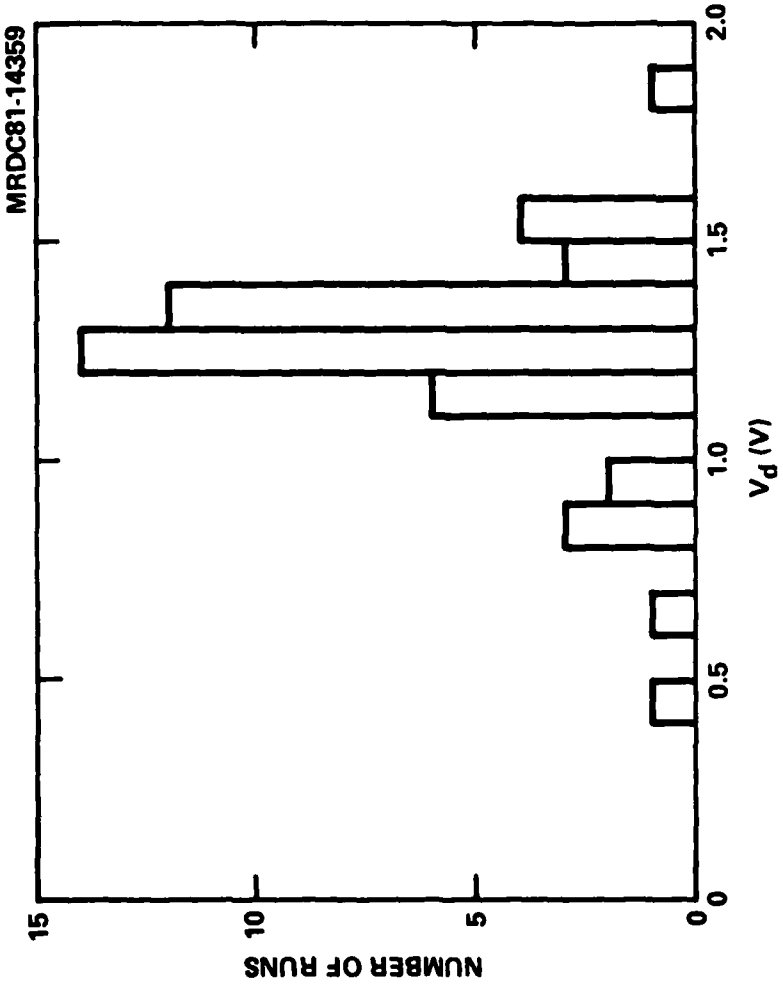


Fig. 4.1-2 Histogram of depletion voltages for a large number of test chips from the same ingot, all processed in identical ways over a period of 9 months.

In order to determine the variations in implant results that are related to substrate material alone, an experiment was conducted in which test chips from a number of different ingots were processed simultaneously. Twelve Bridgman ingots (obtained from Crystal Specialties and Mitsubishi-Monsanto) were represented, as well as twelve LEC ingots (grown at Rockwell). The ingots were preselected according to the standard qualification tests. The distribution of depletion voltage V_d shown in Fig. 4.1-3 was obtained. For the Bridgman materials the standard deviation of V_d was 304 mV (after excluding two of the wafers with anomalously high V_d). The corresponding standard deviation was lower for the LEC ingots, with a value of 170 mV. An even more favorable standard deviation of V_d is observed if the population under test is restricted to those LEC ingots grown after the first 10 runs of the crystal puller. All of the 8 following ingots in the test were nominally undoped and pulled from PBN crucibles. The standard deviation of V_d observed for these 8 ingots was 81 mV.

The measured results indicate that substrate variations have historically been the largest contribution to implant variability, but with LEC material these variations appear to be significantly reduced.

Sources of the variation of threshold voltage among the runs include both process-related and substrate-related effects. As technological improvements are made, variations of V_T on successively finer scales can be extracted from the noise, and the effects of numerous parameters on V_T can be deduced. The effects of several factors such as implant energy, dielectric thickness, impurity contamination, and anneal time on the threshold voltage have been investigated.

The effects of implant energy on the FET threshold voltage for all other parameters remaining constant is shown in Fig. 4.1-4. V_T varies linearly with Se ion energy at approximately 10 mV/KeV. This result is in good accord with expectations, considering the effect of ion energy on channel depth. If a change in Se implant energy leads to a shift in depth δx of each donor in the channel, then the expected change of V_T with energy is

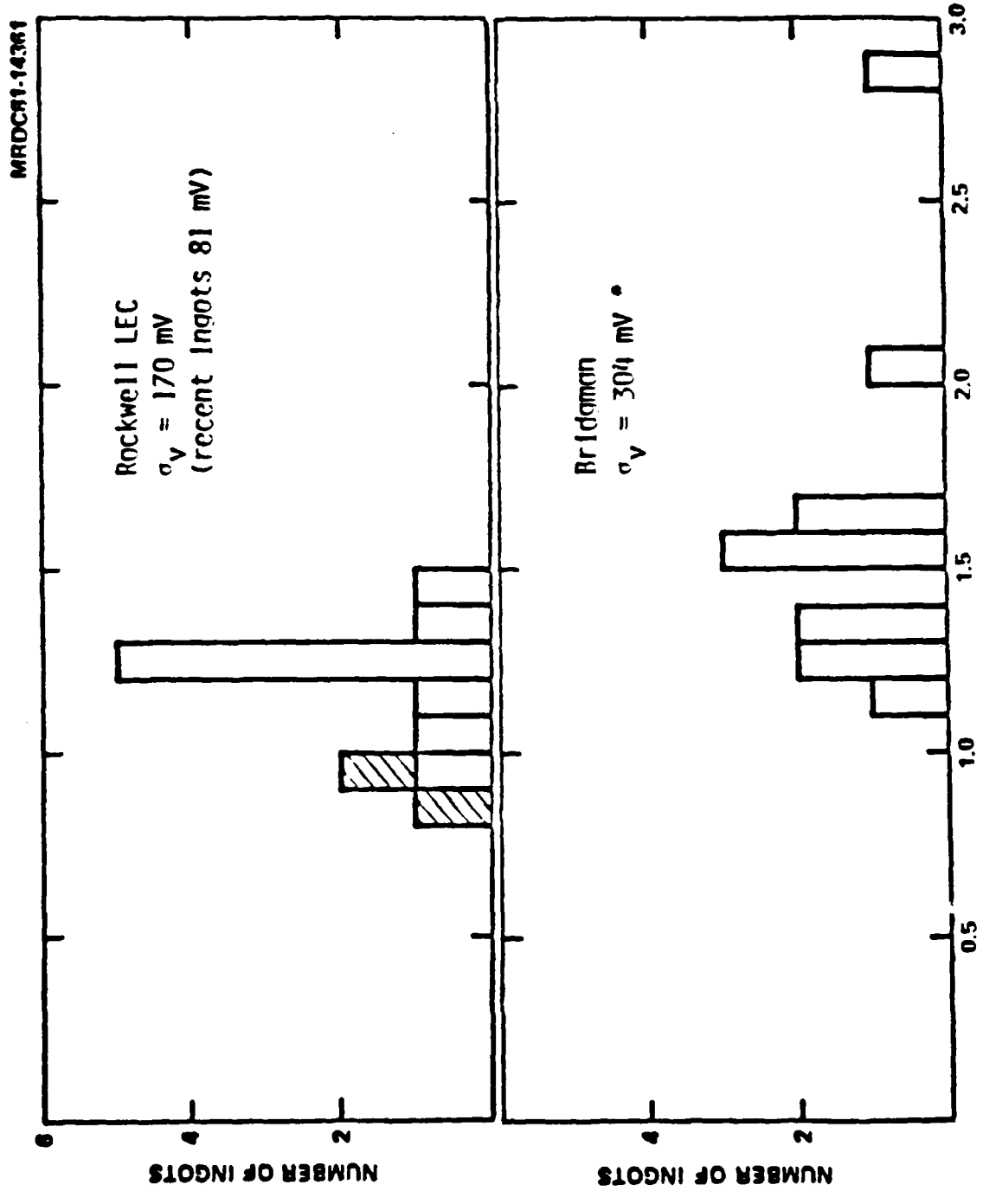


Fig. 4.1-3 Histograms of depletion voltages for a number of test chips from a Bridgman and LEC ingot, respectively. The test chips were all processed simultaneously.

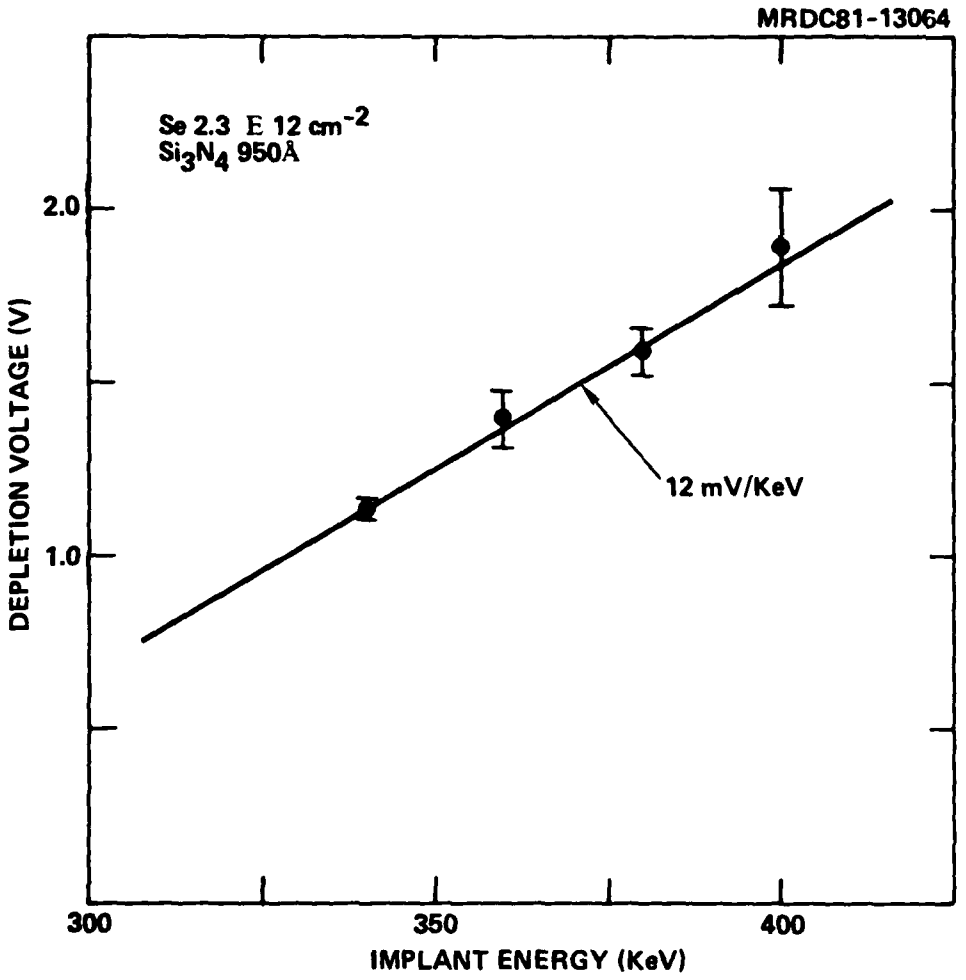


Fig. 4.1-4 Dependence of depletion voltage of Se channel implants on implant energy.

$$\frac{\delta V_T}{\delta E} = \frac{\delta V_T}{\delta x}\frac{\delta x}{\delta E} = \frac{q}{\varepsilon}\phi_{implant}\frac{\delta x}{\delta E} \quad . \qquad (1)$$

Here $\phi_{implant}$ is the total implant dose and $\delta x/\delta E$ is the total stopping power of GaAs for Se ions. Using $\phi_{implant} = 2.3 \times 1^{-12}$ cm^{-2} and a stopping power of 3.45Å/KeV as given by Gibbons et al,[11] the predicted change is 11.4 mV/KeV, in good agreement with experiment. A similar effect is expected for variations in Si_3N_4 cap thickness since in the Rockwell process the cap is deposited prior to implantation. If the stopping power of Si_3N_4 and GaAs are considered to be equal, then the predicted change of V_T with cap thickness is 3.3 mV/Å. This result is again in good accord with experiment, (approximately 3 mV/Å) as shown in Fig. 4.1-5.

The stress produced by the Si_3N_4 cap has been a subject of concern for some time. However, recent measurements indicate that changes in cap stress do nto cause variations in V_T. This result is inherent in the above results where the cap thickness was varied prior to implantation, since the stress imparted to the GaAs surface is directly proportional to cap thickness. To examine this effect further, a series of samples were capped and implanted, and then the cap was thinned substantially (after implantation). As shown in Fig. 4.1-6, the measured V_T for these samples was constant, even though the cap-induced stress varied by up to a factor of 3.

To study the effects of Au, Cu, Ni, Ti contamination, evaporated layers of these metals were deposited on the back sides of test wafers of semi-insulating GaAs. The wafers had been previously encapsulated with sputtered Si_3N_4, and implanted with Se (at a fluence of 2.5×10^{12} cm^2, typical of FET channel layers). The wafers were subsequently annealed at 850°C for 30 min, as used in the IC process. Sealed quarz ampoules were utilized to avoid furnace contamination. After stripping the dielectric encapsulant and carrying out C-V measurements, it was found that the Ni and Ti contaminated samples were comparable to concurrently processed uncontaminated control wafers (having a threshold voltage of -2.0 ± 0.1 V), while there was no discernable implant activation in the Au or Cu contaminated samples. It was of interest

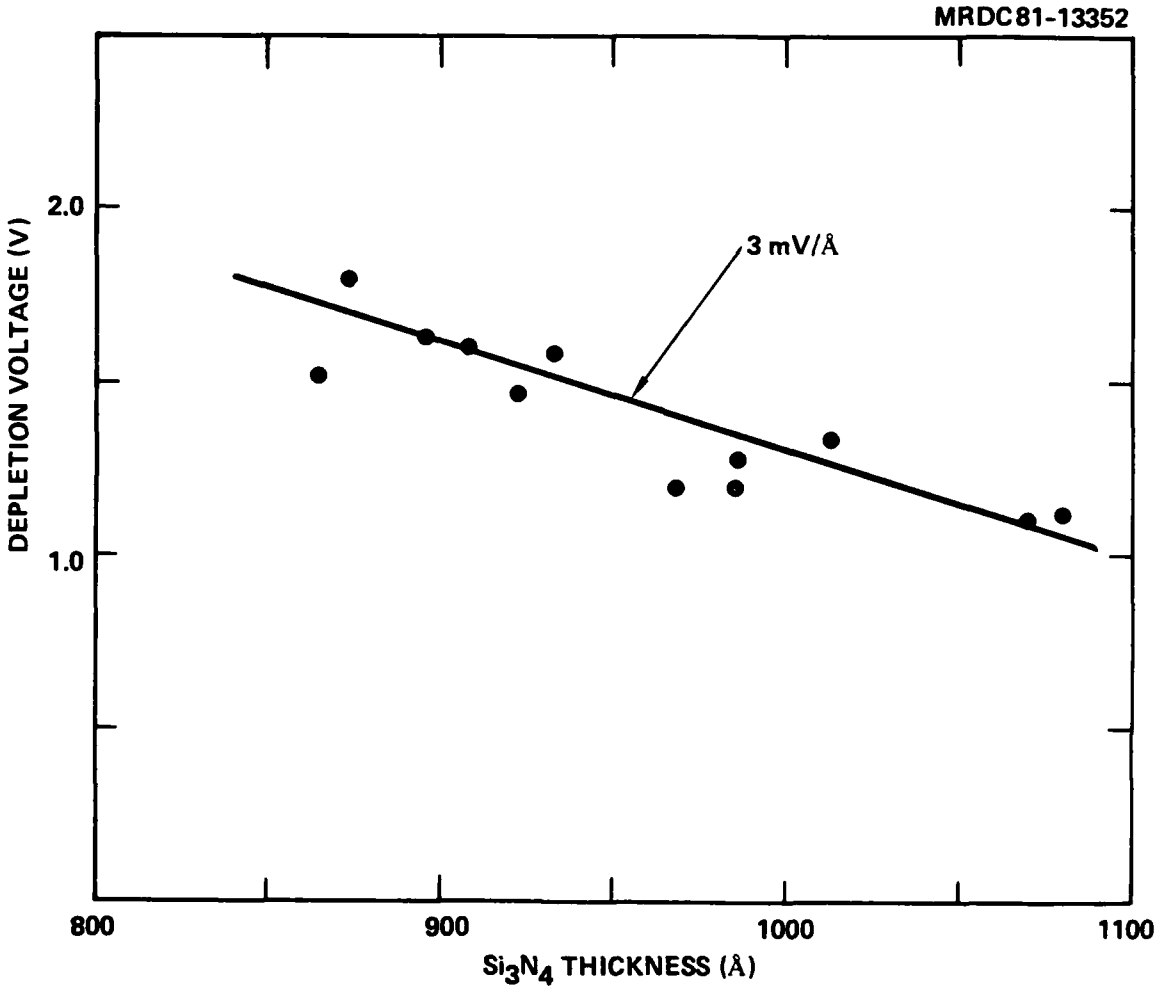


Fig. 4.1-5 Dependence of depletion voltage of Se channel implants on Si_3N_4 thickness prior to implantation.

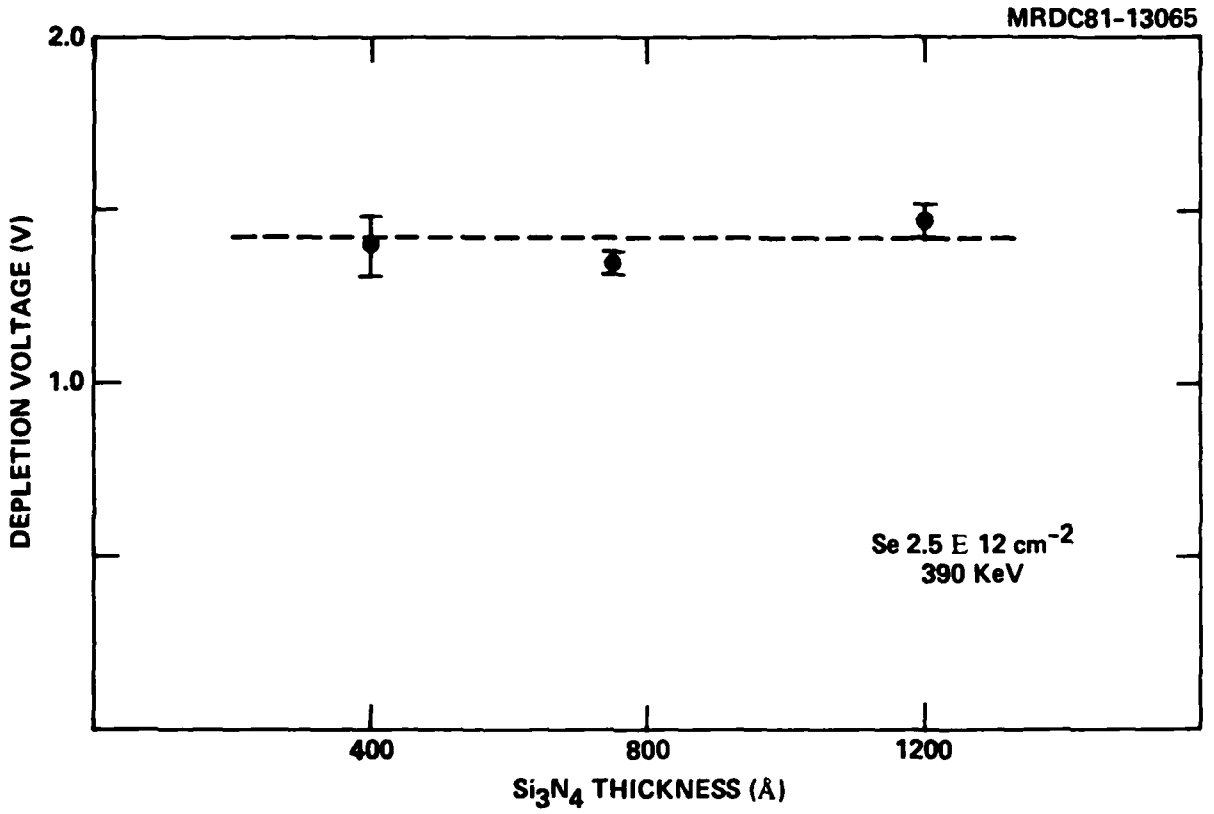


Fig. 4.1-6 Dependence of depletion voltage of Se channel implants on Si_3N_4 thickness during anneal (for constant Si_3N_4 thickness prior to implantation.

to determine if the effects of Au and Cu could be eliminated by protecting the back sides of the wafers with sputtered silicon nitride. Accordingly, samples were processed with evaporated metal layers on the back of wafers encapsulated both front and back. Again, no implant activation was obtained. Apparently these metals can readily diffuse through the cap.

Investigation of silicon contamination of the cap-GaAs interface was undertaken because of the concern that free Si-rich silicon nitride could potentially be formed in the early phases of the cap sputter deposition under some circumstances. To investigate its effects, a silicon layer of the order of 15Å thick was intentionally deposited on test GaAs wafers, and followed by immediate deposition of the standard Si_3N_4 cap without exposing the wafers to air. The silicon deposition was accomplished by sputtering, using a silicon target and argon plasma; a nitrogen plasma was subsequently used to produce the Si_3N_4. The contaminated wafers were implanted with Se, annealed and evaluated in the standard fashion. It was anticipated that an extra donor component would appear due to silicon indiffusion. Unexpectedly, the profiles showed that in addition to the normal Se donor concentration, there was an acceptor-like doping component localized near the GaAs surface, as determined from a reduction in the absolute value of the threshold voltage of about 0.7 V, and an increase in the zero-bias depletion depth of about 600Å. The nature of the acceptor is not known. It may result from an alteration of the GaAs stoichiometry near the surface, if Ga or As preferentially interacts with the silicon-rich interfacial layer.

Variations of depletion voltage with the anneal time were also investigated. Test chips of Cr doped or undoped semi-insulating GaAs were capped, Se-implanted and then annealed for varying periods of time at 850°C. C-V measurements were then done to determine carrier profiles and depletion voltages, V_d. The carrier profiles for long anneal times showed increase depth and lower peak carrier densities compared with the standard 30 minutes as qualitatively expected for Se diffusion.

Significant activation was found for anneals as short as 8 minutes. The variation of V_d with anneal time is shown in Fig. 4.1-7. It is apparent that V_d is quite sensitive to the time in the range below 30 minutes, suggesting that the current process represents a good compromise between limiting diffusion and avoiding significant V_d variations. No significant difference was found between the behavior of Cr doped and undoped LEC substrates, indicating that the changes in V_d from Cr diffusion occur rapidly (in less than 5 minutes), and then saturate due to Cr depletion, so that further changes are apparently related only to Se diffusion.

4.2 Evaluation of a 3-Implant Process

Two implantations are normally used in the Rockwell fabrication process for digital IC's. One implant (called n^-) is used to form the FET channels, and the other (called n^+) to form the cathodes of the logic diodes. Both implants are superimposed in ohmic contact regions to obtain low sheet resistance in those areas. Since implantations are done prior to any other fabrication step, there is no obstacle to using more than two implants. Experiments were undertaken to determine whether an additional implant (called n^{++}) in the ohmic contact regions might lower the contact resistance.

In this experiment, silicon used for both the n^+ (second) and n^{++} (third) implant in order to avoid mixing of implant species and recognizing that silicon implants result in high electrical activations.[14] Processing proceeded in a normal manner with the addition of the higher dose silicon implant ranging from 3.8×10^{12} cm^{-2} to 10^{14} cm^{-2}. This implant was masked using the ohmic contact mask, therefore allowing only the local regions under the ohmic contacts to be heavier doped. One-inch square wafers were implanted with various doses over 4 quadrants so that variations of contact resistance could be compared with variations of sheet resistance on the same wafer.

The additional n^{++} implant processing was conducted without difficulty. This indicates that implants through the cap (Si_3N_4) up to doses of 10^{14} cm^{-2} can be accomplished without any detrimental effects resulting from

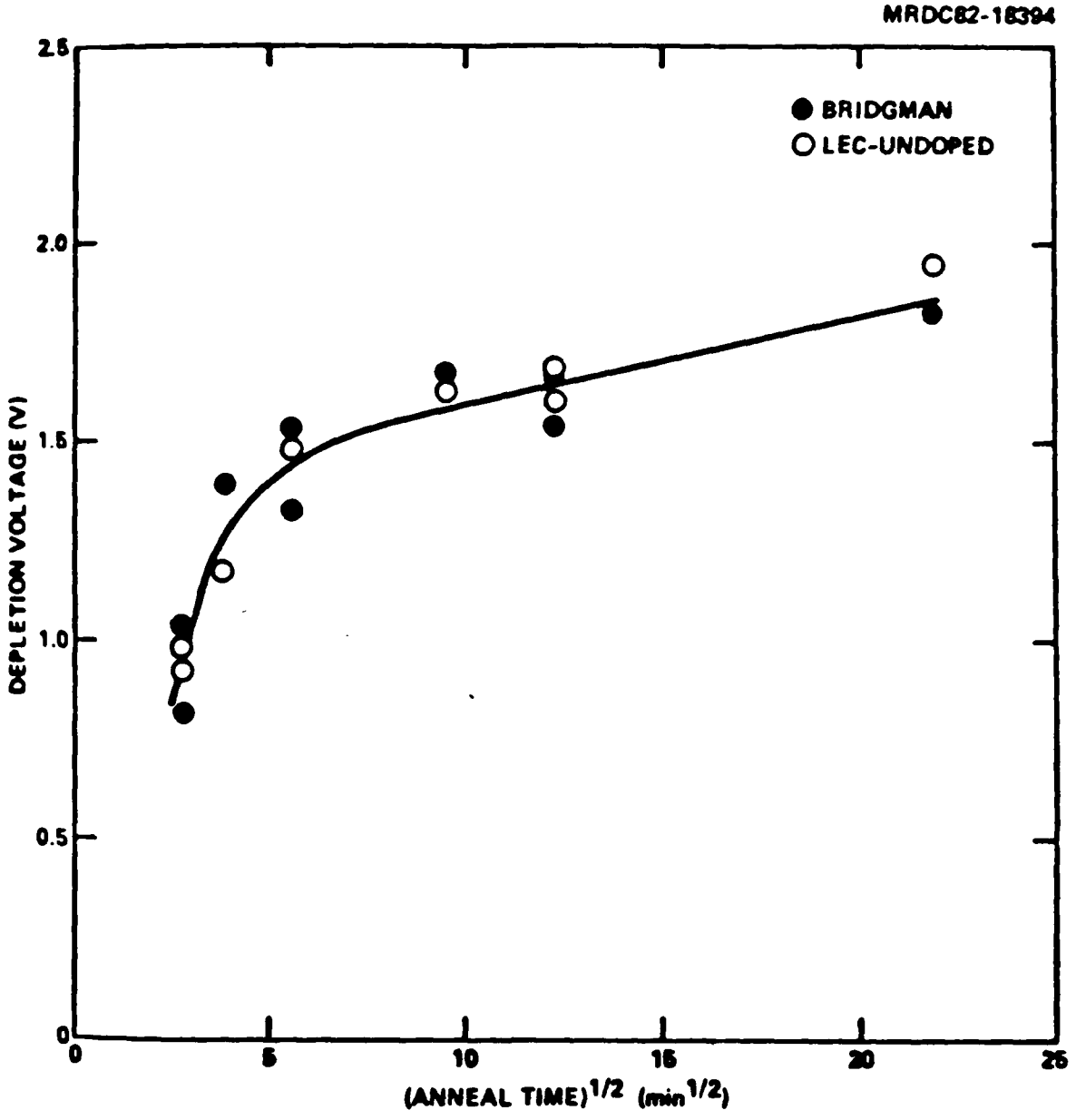


Fig. 4.1-7 Depletion voltage of Se implanted wafers (at a dose of 2.5 x 10^{12} ions/cm^{-2}) as a function of the anneal time. The implants were made in semi-insulating GaAs substrates. The annealing cap consisted of sputtered Si_3N_4.

ion damage of the dielectric. Table 4.2-1 compares the silicon dose and corresponding measured sheet resistance for 4 different implant regions on two separate wafers with the measured specific contact resistance (r_c). The specific contact resistance and the sheet resistivity measurements were obtained from 72 ohmic contact transmission line method[14] test structures evenly distributed across each IC wafer. Each separate area of the wafer thus allows 18 data points to be collected.

Several conclusions can be drawn from the above data. First, the sheet resistance resulting from a room temperature Si implantation for doses up to 10^{14} cm^{-2} using a Si_3N_4 cap and 850°C arnealing saturates at a value of

Table 4.2-1

Sheet Resistance and Specific Contact Resistance(r_c) vs Silicon Implant Dose on Two GaAs IC Wafers

	Dose: 3.38×10^{13} cm^{-2}		Dose: 10^{14} cm^{-2}
Wafer (A) *	$\bar{\rho}_s$ = 76 Ω/□ $\bar{r}_c = 1.72 \times 10^{-6}$ Ω cm^2	(A)	$\bar{\rho}_s$ = 58 Ω/□ $\bar{r}_c = 1.94 \times 10^{-6}$ Ω cm^2
(B)	$\bar{\rho}_s$ = 77 Ω/□ $\bar{r}_c = 1.16 \times 10^{-6}$ Ω cm^2	(B)	$\bar{\rho}_s$ = 57 Ω/□ $\bar{r}_c = 1.13 \times 10^{-6}$ Ω cm^2
	Dose: 3.8×10^{12} cm^{-2}		Dose: 7×10^{13} cm^{-2}
Wafer (A)	$\bar{\rho}_s$ = 455 Ω/□ $\bar{r}_c = 1.87 \times 10^{-6}$ Ω cm^2	(A)	$\bar{\rho}_s$ = 62 Ω/□ $\bar{r}_c = 1.92 \times 10^{-6}$ Ω cm^2
(B)	$\bar{\rho}_s$ = 452 Ω/□ $\bar{r}_c = 7.94 \times 10^{-7}$ Ω cm^2	(B)	$\bar{\rho}_s$ = 57 Ω/□ $\bar{r}_c = 1.22 \times 10^{-6}$ Ω cm^2

*Each value is the average of 18 data points.

~ 60 Ω/□. It is estimated from earlier Si implantation profile studies that a peak carrier concentration of ~ 10^{18} cm^{-3} can be expected from this process. It is well known from past work that Si implant activation levels go down with increasing implant dose, and that continuing to increase the dose does not necessarily result in higher levels of carrier concentrations with the present cap and anneal conditions. Thus, it is not surprising that a dose of 7×10^{13} cm^{-2} resulted in a similar sheet resistance (~ 60 Ω/□) as a 10^{14} cm^{-2} dose. Even the 3.38×10^{13} cm^{-2} dose level yields a respectable 76 -77 Ω/□ sheet resistance. In general, the lowest ρ_s values observed using this process at this laboratory has been ~ 40 Ω/□ for higher doses and higher anneal temperatures (900°C). A dose of 3.8×10^{12} cm^{-2} (~ 450 Ω/□) was included in these experiments to simulate the normal implant dose conditions used in the current process to compare with the higher doping levels under investigation. In all of the implant regions the average value of r_c was measured to be ~ 1×10^{-6} Ω · cm^2. The specific contact resistance measurements on these wafers clearly indicate that using a high quality ohmic contact process over a sheet resistance range of 60-450 Ω/□ results, at least initially (as processed) in similar ohmic contact resistance.

The experiment on a third, n^{++}, implant was completed by observing the correlation between circuit switching speed and doping density under ohmic contact regions. Nine-stage ring oscillators were fabricated on the wafer that was partitioned in four quarters, with each quarter of the wafer receiving separate n^{++} Si implantation doses. The data presented in Table 4.2-2 represent a summary of ring oscillator performance for these four different areas. It can be seen that the frequency of operation increases when the sheet resistance is decreased. A range of ρ_s from 57 to 453 Ω/□ results in maximum oscillation frequencies of 360 MHz (τ = 154 ps) and 255 MHz (τ = 218 ps), respectively. The overall ring oscillation speeds are very modest due to the exceptionally low threshold voltage MESFETs used in this experiment. However, propagation delays in the 150-200 ps region are quite good considering the associated low power dissipation, providing speed-power products of 24-27 fJ. The scaling of propagation delay with n^{++} doping level will

more strongly dominate in a circuit employing low threshold MESFETs circuit (~ 0.6V) such as the one tested, as opposed to the more typical, ~ 1.0 V, MESFETs thresholds used for SDFL. This is because reducing source resistance is comparatively more important in MESFET devices with higher channel sheet resistances.

Table 4.2-2

Ring Oscillator Performance vs
Sheet Resistance in the Ohmic Contact Region

Wafer Location	$\rho_S(\Omega/\square)$	*f(MHz)	τ(ps)	Gate Parameters P(μW)	**Pτ(fJ)
Q3	453	255	217.8	123	26.8
Q2	76	295	188.3	127.4	24
Q4	60	302	183.9	141.6	26
Q1	57	360	154.3	171.4	26.4

*Ring oscillators biased for maximum operating frequency.
**The very low speed power products are a result of having very low threshold voltages ($\bar{V}_T$ = 0.577 V) on the 10 μm wide MESFETs.

In conclusion, the addition of a third implant in the ohmic contact regions of the devices showed only modest advantages. Although it was proved that an additional implant step could be easily incorporated in the fabrication process, the additon of any lithography step is bound to cause some loss of yield. The benefits in terms of performance do not seem to justify adding the third implant to the standard fabrication process.

4.3 Metallization Yield

Analysis of test results from the 8 x 8 bit parallel multiplier circuit (1008 gates)[1] indicated that one of the main factors limiting the functional yield of this circuit was the appearance of electrical shorts between power supply lines. Out of a total of 960 multipliers tested, 599 (62%) were

found to have shorted power supply lines. Assuming that this problem was not associated with shorts in the active devices, or isolation failures, it must be attributed either to failure of crossover of second over first level metal, or to shorts between two adjacent power supply lines (SDFL power supply lines are mainly designed as part of the second-level interconnects). The planar crossover techniques used in this work have, inherently, very high yield. Recent evaluation has verified this premise. A large number of crossover test structures containing 9,000 crossovers per structure, evaluated on 6 randomly chosen wafers yielded 86% (248/288) fully functional structures with a ± 8 V test voltage applied between first and second level metal interconnects. This is a good result considering that every structure on each wafer was measured, and no effort was made to pre-screen wafers that were thought to have better lithographic yield. Furthermore, at least one wafer exhibited 100% yield corresponding to 432,000 isolated crossover structures on that wafer.

Without any other indication to the contrary, it appeared that shorts between adjacent second-level metal power supply lines were responsible to a large degree for the limited yield observed on the 8 x 8 multipliers. It should be stressed that this is a first order lithography yield limitation, which must be improved before additional device and circuit yield analysis can be performed. Good yield on the second level interconnects is a necessary, but not sufficient condition for successful operation of these LSI chips.

Since the overall test results of the 8 x 8 multipliers showed that 62% of the circuits suffered from shorts, a thorough visual inspection of every 8 x 8 multiplier die was conducted on 5 wafers. The three major defects observed were: nonuniformity of metal thickness (evaporation splattering); photoresist residue; and random dust or particles. Table 4.3-1 contains the results of this visual inspection showing the relative percentage of each type of defect. The conclusion from Table 4.3-1 is that second level metal splattering is one of the key problems. Table 4.3-2 contains a summary of visually defective dies for both first (SM) and second level metal (2M) defects. The table shows that the total number of shorted circuits 97/160 (61%) on these 5

Table 4.3-1

Classification of Second Level Interconnect Defects*

Wafer	TYPE OF DEFECT		
	Metal Splatter	Photoresist Residue	Random Particle
AR5-22	10	12	6
AR5-23	5	10	5
AR5-51	6	12	4
AR5-61	24	6	4
AR5-81	15	2	12
	45% (60/133)	32% (42/133)	23% (31/133)

*Total number of defects observed, eventually more than one per circuit.

Table 4.3-2

Summary of Visual Inspection for First (SM) and Second (2M) Metal Interconnect Defects

	ELECTRICAL TEST	VISUAL INSPECTION OF MULTIPLIER CIRCUITS		
Wafer	Shorted Devices/ Total Devices	Number SM Defects*	Number 2M Defects**	Number Both 2M, SM
AR5-22	24/32	9	25	4
AR5-23	10/32	11	7	2
AR5-51	11/32	8	17	7
AR5-61	30/32	5	30	4
AR5-81	22/32	8	24	3
	61%(97/160)	26%(41/160)	64%(103/160)	13%(20/160)

*Regardless of 2M defects
**Regardless of SM defects

wafers is representative and in good agreement with the 62% electrical failures observed for all of the processed 8 x 8 multiplier wafers. As indicated in Table 4.3-2 the largest number of defects (64%) was found on the second level metal, with only 26% of the die showing first level metal defects. A small percentage of the dies, 13%, had simultaneous first and second level metal defects. In summary, the data collected from wafers with 8 × 8 multipliers date indicate that the first order defects on the 8 x 8 multiplier circuits are in the second level interconnects. Efforts to improve the second level metalization and interconnect are discussed in the rest of this section.

Second Level Metallizations

The second level interconnects are defined by ion milling, where energetic ions bombard the surface and sputter atoms from it. Over etching is the method used to insure complete removal of the desired material. However, overetching is not adequate for completely removing all the material from areas where the metal thickness is much greater than the average (splattering), or from areas which have foreign materials such as photoresist residues or dust particles. Incompletely etched metal can result in defective shorted patterns, and it can lead to problems such as shorted power supply lines.

The second level metalization was deposited by e-beam evaporation. An appealing alternative deposition technique, magnetron sputtering, was investigated. Magnetron sputtered films have excellent via step coverage and do not exhibit any splattering. The magnetron sputtering system used for these experiments was equipped with a planetary fixture allowing films to be deposited with ±3% thickness uniformity. However, this system, with a small (~ 4") target and a large planetary, deposits films of rather high resistivity. Because of the mechanism of the planetary, the substrate is traveling in and out of the deposition zone, allowing Ar atoms to be trapped in the successive layers of deposited material, thereby increasing the resistivity of deposited films. The bulk resistivity of Au films deposited by magnetron sputtering is 0.040 Ω-μm, which is 1.7 times higher than films deposited by e-beam evapora-

tion (0.0235 Ω-μm). This disadvantage of the magnetron sputtered films was later reduced with the installation of a system compatible with 3 inch diameter wafers.

To evaluate the improvements of second level metal process, a yield test mask set was fabricated. The mask had two sets of inter-digitated lines which can be electrically tested for shorts between two adjacent lines. A sketch of the test structures is shown in Fig. 4.3-1. The mask set has both light field and dark field versions so that it be can be used both with ion milling and lift-off techniques. A photomicrograph of part of the test structure is shown in Fig. 4.3-2. Pattern A has 3 μm lines with 2 μm spacing, and pattern B has 8 μm lines with 2 μm spacing. The length of each parallel line is 1200 μm. Both patterns A and B have separated test sets which can be independently analyzed. The total length of adjacent lines in a set starts with 12,000 μm and increases by doubling up to 144,000 μm. There are two pairs of pattern A and B in each chip of 2.7 x 2.7 mm; 72 pairs in a 25 x 25 mm wafer.

A direct comparison using the test mask described above indicates that the yield of long parallel lines resulting from E-beam evaporation is much lower than the yield resulting from magnetron sputtering as shown in Fig. 4.3-3. As the figure indicates, the yield for magnetron sputtering is 3 to 4 times higher than the best yield obtained by E-beam evaporation. The lower yield obtained by E-beam evaporation is attribued to the splattering occurring during evaporation.

In order to minimize splatter from evaporation, the evaporator used for this experiment was upgraded so that the E-beam could be swept over the Au source. However, the yields resulting from wafers deposited by this system (shown by triangles on Fig. 4.3-3) were still lower than those from magnetron sputtering (squares on Fig. 4.3-3) while being more reproducible. The data base was expanded by evaluating wafers on which Au was deposited by two evaporators used for other GaAs programs. It was found that the wafers processed with the standard IC evaporation equipment had better yields. The points in the Fig. 4.3-3 represent averages over the following data base:

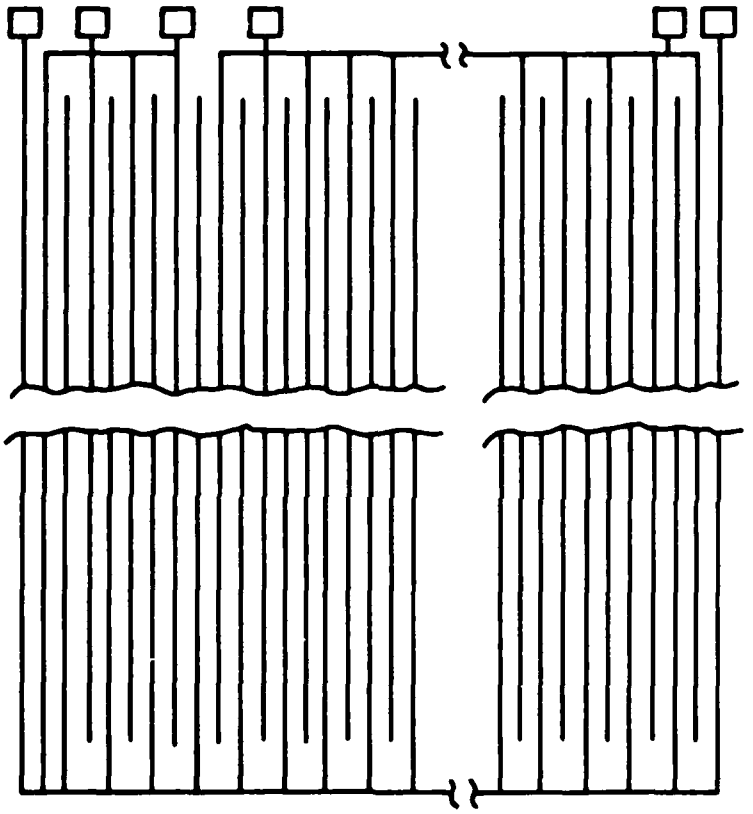


Fig. 4.3-1 Schematic of second level interconnects yield test structure.

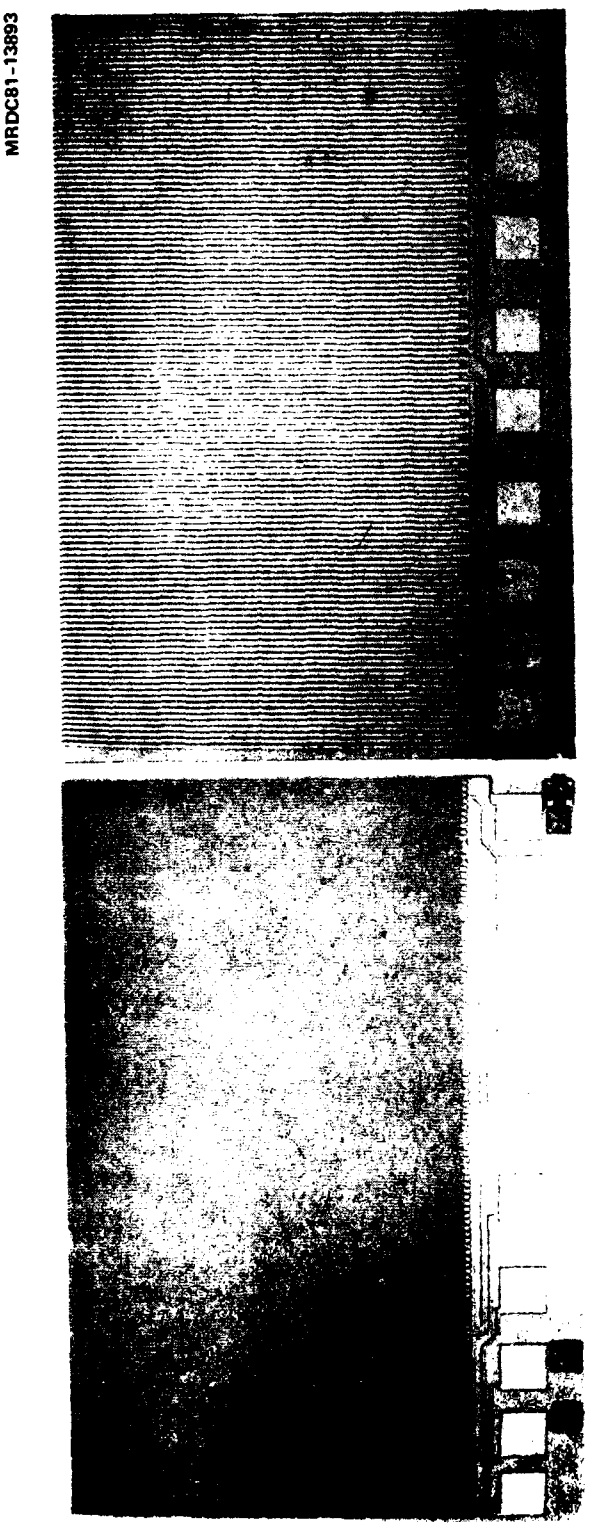


Fig. 4.3-2 Photomicrograph of part of the second level interconnects yield test structure.

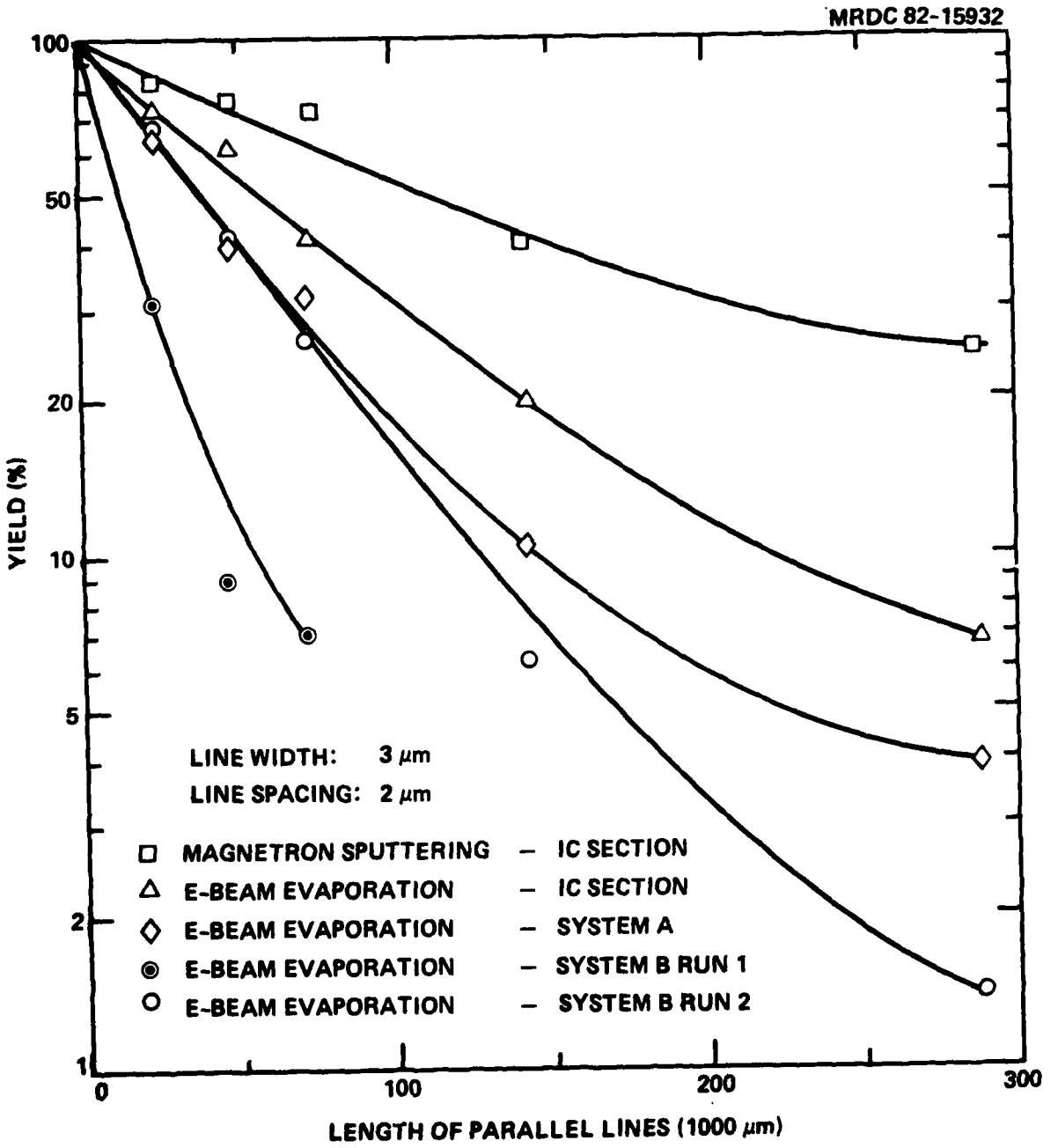


Fig. 4.3-3 Yield of parallel second level metal lines fabricated using several different metal deposition systems. The lines were defined by ion milling.

Magnetron Sputtering	- IC Equipment	2 runs, 4 wafers/run
E-Beam Evaporation	- IC Equipment	2 runs, 4 wafers/run
E-Beam Evaporation	- System A	1 run, 4 wafers/run
E-Beam Evaporation	- System B, Run 1	1 run, 2 wafers
E-Beam Evaporation	- System B, Run 2	1 run, 2 wafers

In conclusion, magnetron sputtering resulted the best metal deposition technique for second level interconnects, and it was adopted as the standard technique in our fabrication line. Although some improvements in specific resistivity are desirable, the current resistivity values are quite acceptable, and they are taken into account in the design.

Multi-Level Interconnects

As the complexity and size of the integrated circuits increase, the number of multi-level interconnects and crossovers increases dramatically. Therefore, the integrity and yield of crossover structures and multi-level interconnects is an important factor for successful LSI/VLSI fabrication. The yields of crossover structures were discussed earlier in this section. Here, the results from the evaluation of the yield of long chains of interconnects, are presented.

The interconnect test structure used in this study consists of a chain of first to second level metal interconnects. A drawing of the cell used to build the long chain is shown in Fig. 4.3-4. Alternating short strips of Schottky (first level) metal and second level metal are interconnected through via holes. To save space on the wafers, the interconnect test structure was laid out as a long meander in the kerf lines. A portion of the pattern is shown in Fig. 4.3-5. The total length of the pattern includes 14878 interconnects. Note, as a reference, that an 8 × 8 multiplier (1000 gates circuit) has ~ 7000 interconnects. The interconnect pattern has taps at intermediate points so that yield can be measured for several lengths of the chain.

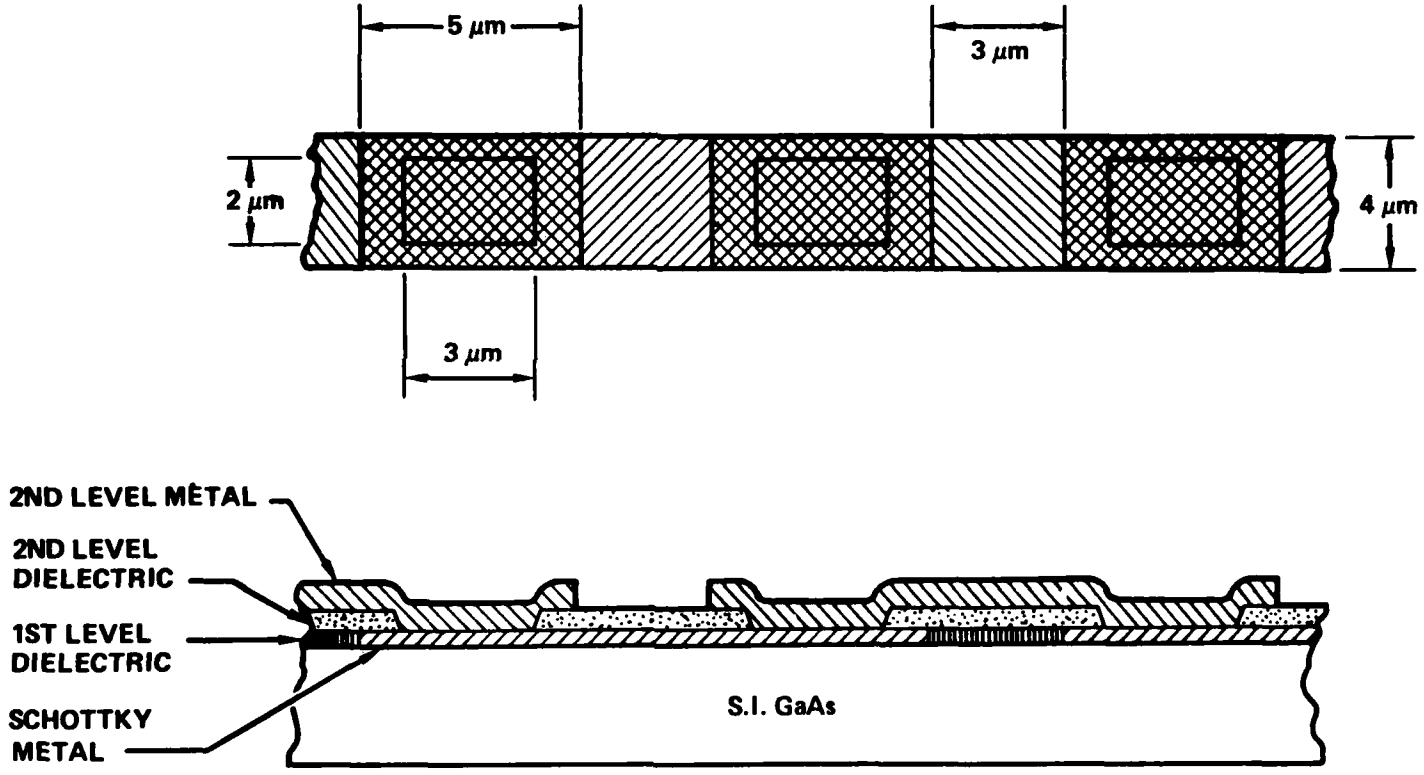
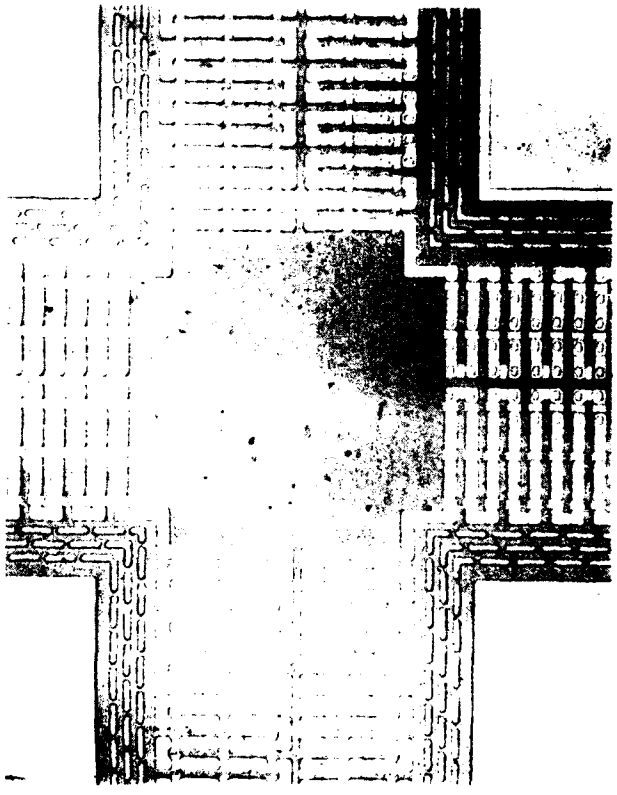


Fig. 4.3-4 Schematic of the cell used to build a long chain of first/second level interconnects.

MRDC81-14303



VIA SIZE: 2 x 3 μm
TOTAL NUMBER OF VIAS: 14,878
VIA RESISTANCE: 0.077Ω/VIA
YIELD: 4,162 VIAS – 83.5% (20 WAFERS TESTED)
14,878 VIAS – 62.5% (20 WAFERS TESTED)

Fig. 4.3-5 Portion of the long meander forming the interconnect integrity test structure.

The integrity of the interconnects was electrically tested by injecting a current of 4 mA through the string. The test can only determine if a string of interconnects is continuous (has current flow) or broken (has no current flow). The test cannot indicate if any elements in the string are shorted together unless a long chain of the string is shorted so that an abnormally low resistance is observed.

The yields obtained are indicated in Fig. 4.3-6. They represent the averages obtained from 20 wafers. The yield of 400 interconnects is 100%. It decreases slowly to ~ 65% for the maximum number (14878) of interconnects. The interpolated yield for 7000 interconnects, the number in the 8 × 8 SDFL multiplier, is slightly over 80%. This is a satisfactory number today. However, further improvements will be needed for higher circuit complexity.

The average resistance of each via is 0.077 Ω, which is approximately equal to the resistivity of a square of 3000Å thick Au Schottky metal (0.078 Ω/□). This value is low enough because it means that the interconnect resistance is negligible with respect to the line resistance. From a process standpoint, this low value indicates that the surface of the Schottky (first level) metal inside the vias are clean after via window etching, and the second level and first level metal make very good contact.

4.4 Fabrication of 1-inch Wafers

Seven lots (of 4 wafers each) were processed using mask set AR6 (see Sec. 5 for a description of the circuits on this mask set). All the wafers were characterized by our standard parametric test procedure based on the automatic test of arrays of test structures placed on all wafers.

A sample of such parametric data is shown in Figs. 4.4-1 and 4.4-2. The data in Fig. 4.4-1 represent a histogram of threshold voltages for the 48 test FETs (50 μm channel width, 1 μm gate length) distributed across the 1 inch square wafer. A wafer map is shown on the left. The average threshold voltage, V_p = -1.02 V is within the desired range of 0.9-1.3 V, and the wafer standard deviation of 72 mV is quite typical (best values are ~30 mV). A

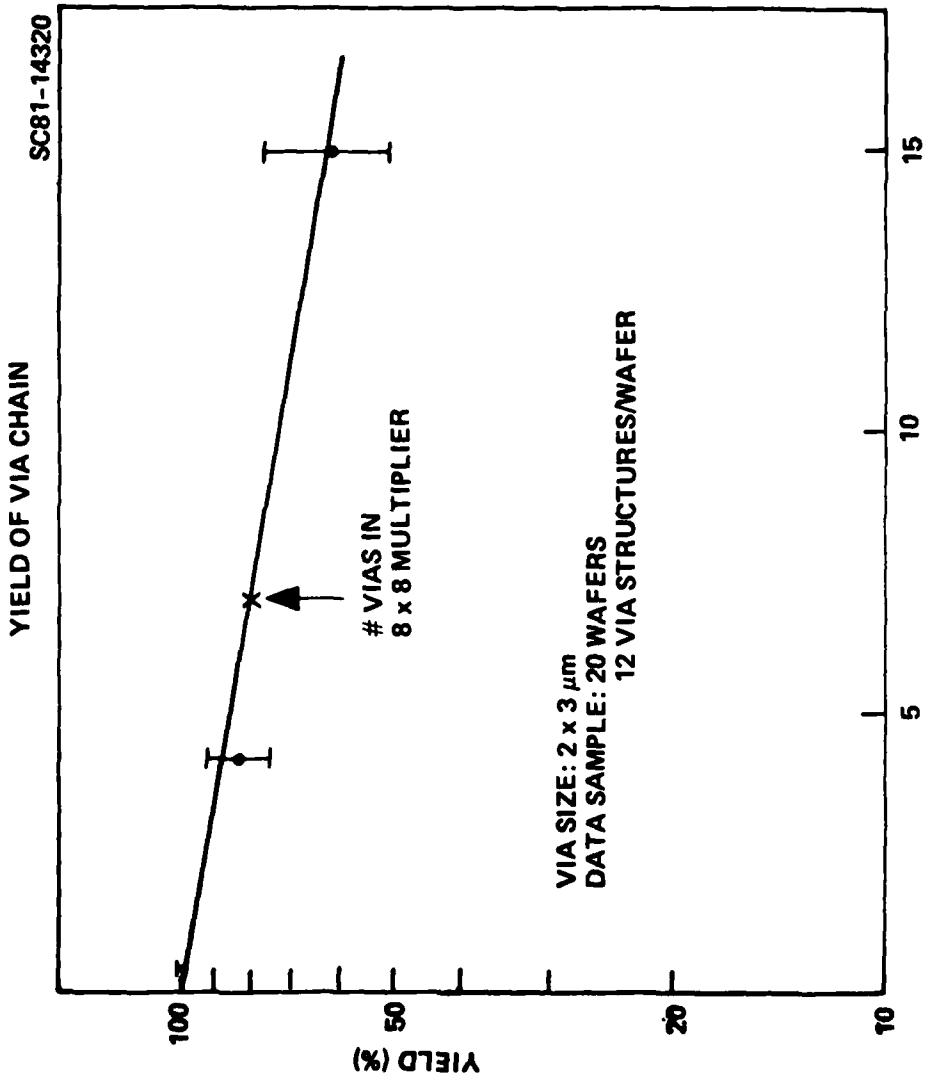


Fig. 4.3-6 Yields of first/second level interconnects.

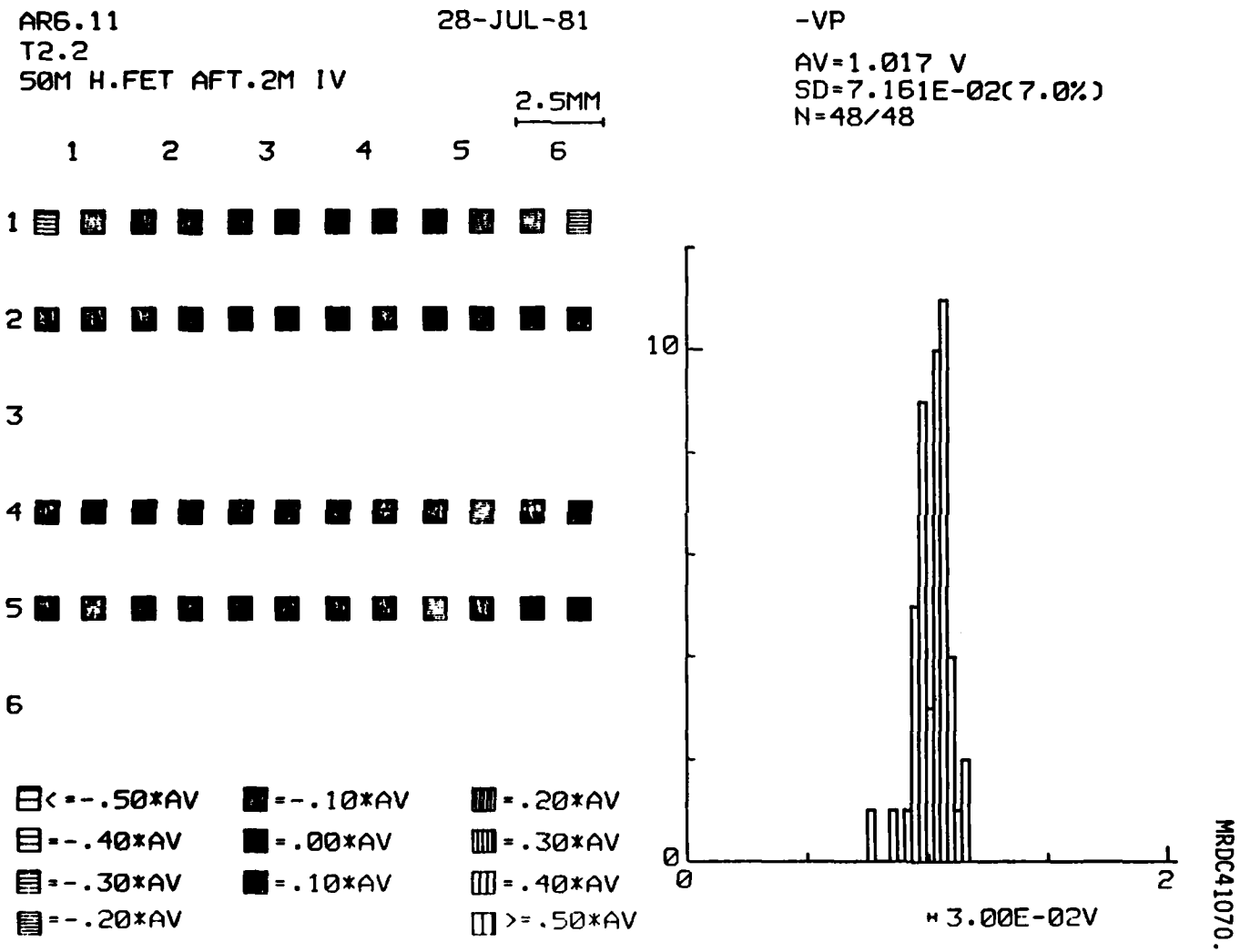


Fig. 4.4-1 Wafer map and histogram of test FET threshold voltages ($-V_p$) from a typical AR6 wafer.

Rockwell International

AR6.11
T2.2 28-JUL-81
50M H.FET AFT.2M IV

PARAM.	UNIT	AVERAGE	SD	%
-VP	V	1.017	7.1613E-02	7.0
RS	OHMS	47.40	13.58	28.6
K	MMHO/V	4.047	.9966	24.6
-VPE	V	.5811	4.8636E-02	8.4
IDSS	MA	3.055	.3676	12.0
GD	MMHO	.1128	2.9177E-02	25.9
RON	OHMS	184.3	22.15	12.0
VSAT	V	1.009	.1039	10.3
IG	NA	9.500	7.366	77.5

TOTAL: 48
WORK : 48 (100.0%)

Fig. 4.4-2 Statistics of FET parameters from a typical AR6 wafer.

complete summary of parametric data from the same array of FETs is shown in Fig. 4.4-2. Here the averages and standard deviations of all the parameters needed to characterize the devices are printed. Most important among these parameters are the threshold voltage, V_p, the saturation current, I_{dss}, the "on" resistance R_{ON}, and constant K in the equation used to model the saturation region of the characteristics,

$$I_{ds} = K(V_{gs} - R_s I_{ds} - V_p)^2 \quad . \tag{1}$$

The average values and standard deviations in Fig. 4.4-2 are quite typical for 50 μm wide FETs, and the parameters which are width dependent scale well with the width. These data contribute to the data base from which SPICE circuit simulation parameters are extracted and updated.

Figures 4.4-3 to 4.4-5 display the average value of some key parameters as a function of time for all the AR6 wafers. In these three figures, the horizontal scale represents the date on which the data were taken. Each point corresponds to the average value over one wafer of the parameter displayed on the plot. Figure 4.4-3 corresponds to threshold voltages, which fall in the -0.9 to 1.3 V range, with few exceptions. Figure 4.4-4 corresponds to the specific resistance of the ohmic contacts, which is near 10^{-6} Ω-cm^2 for the majority of the wafers. Finally, Fig. 4.4-5 corresponds to the series resistance of the logic diodes, which all fall in the desired $R_S <$ 800Ω range, with most wafers below 500Ω. Other characterization measurements not discussed here include verification of carrier concentration profiles, and verifications of metallization and interconnect resistance and crossover capacitances.

The above results are quite satisfactory. Table 4.4-1 contains a summary of the parametric test results. Of 25 wafers on which fabrication was completed (89% of the starts), 20 (80%, or 71% of the total) exhibited a threshold voltage within the acceptable range, and were considered acceptable for circuit testing.

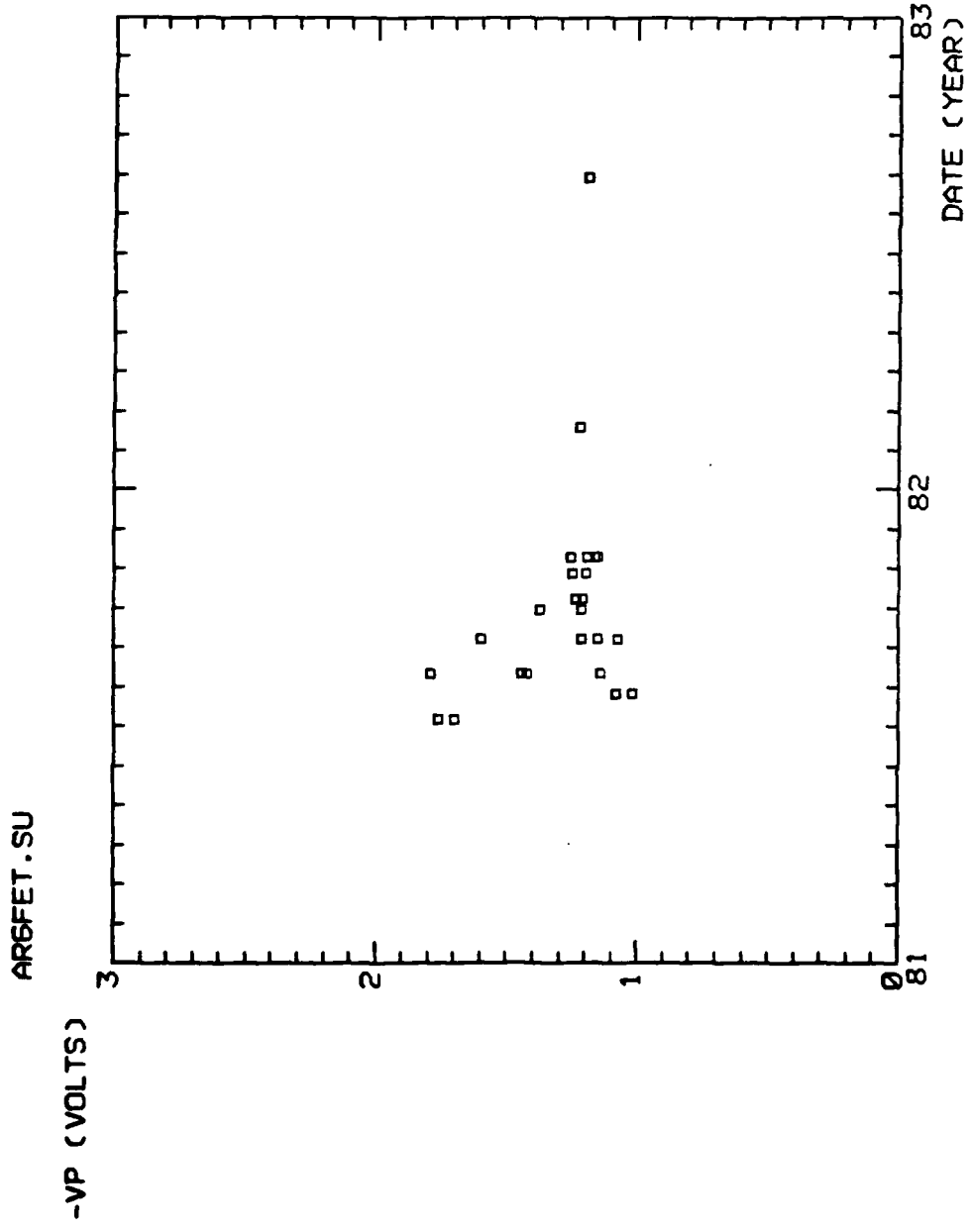


Fig. 4.4-3 History of average of threshold voltges, V_p, for the AR6 wafers. Each data point represents the mean for one wafer.

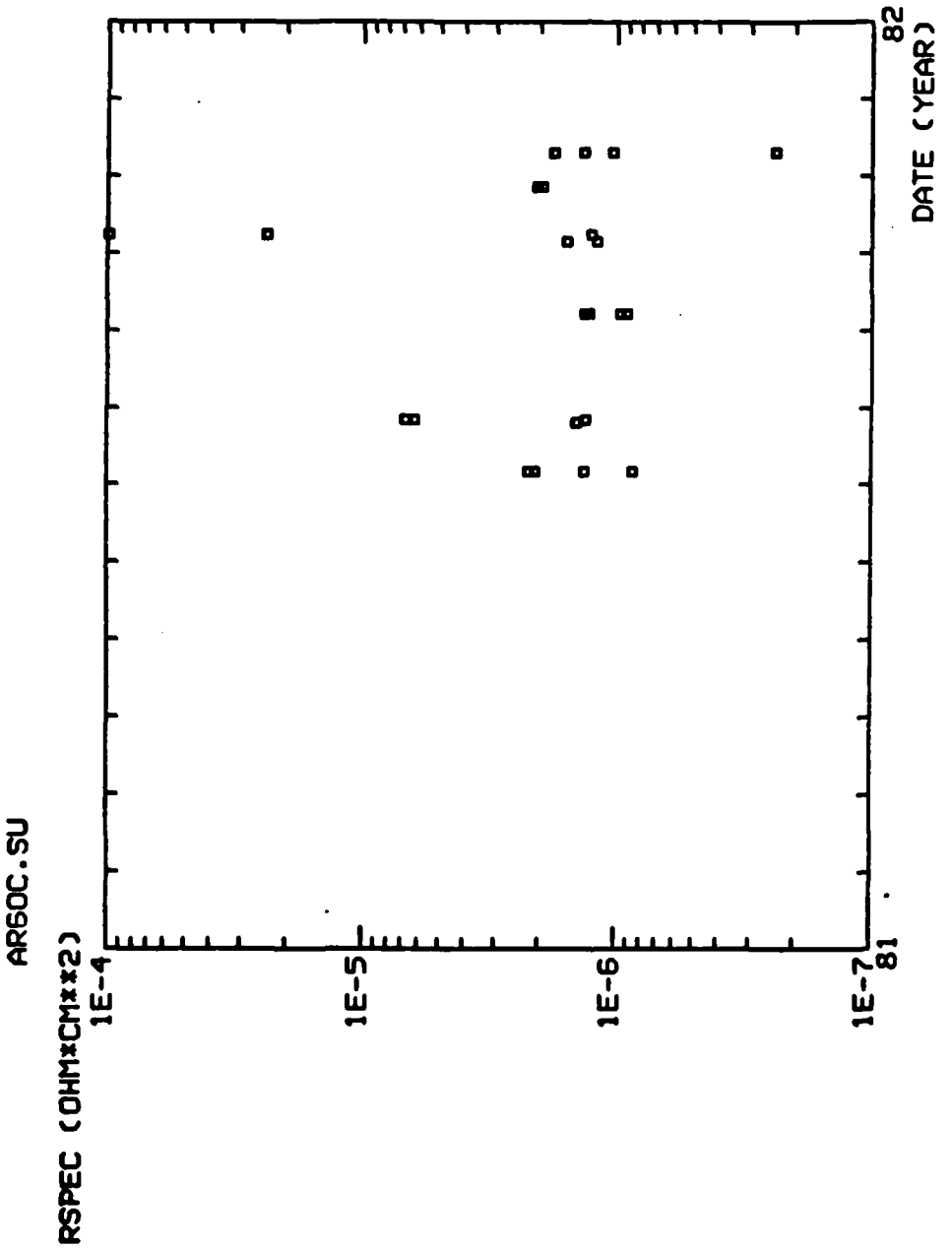


Fig. 4.4-4 History of ohmic contact specific resistance for the AR6 wafer. Each data point represents the mean for one wafer.

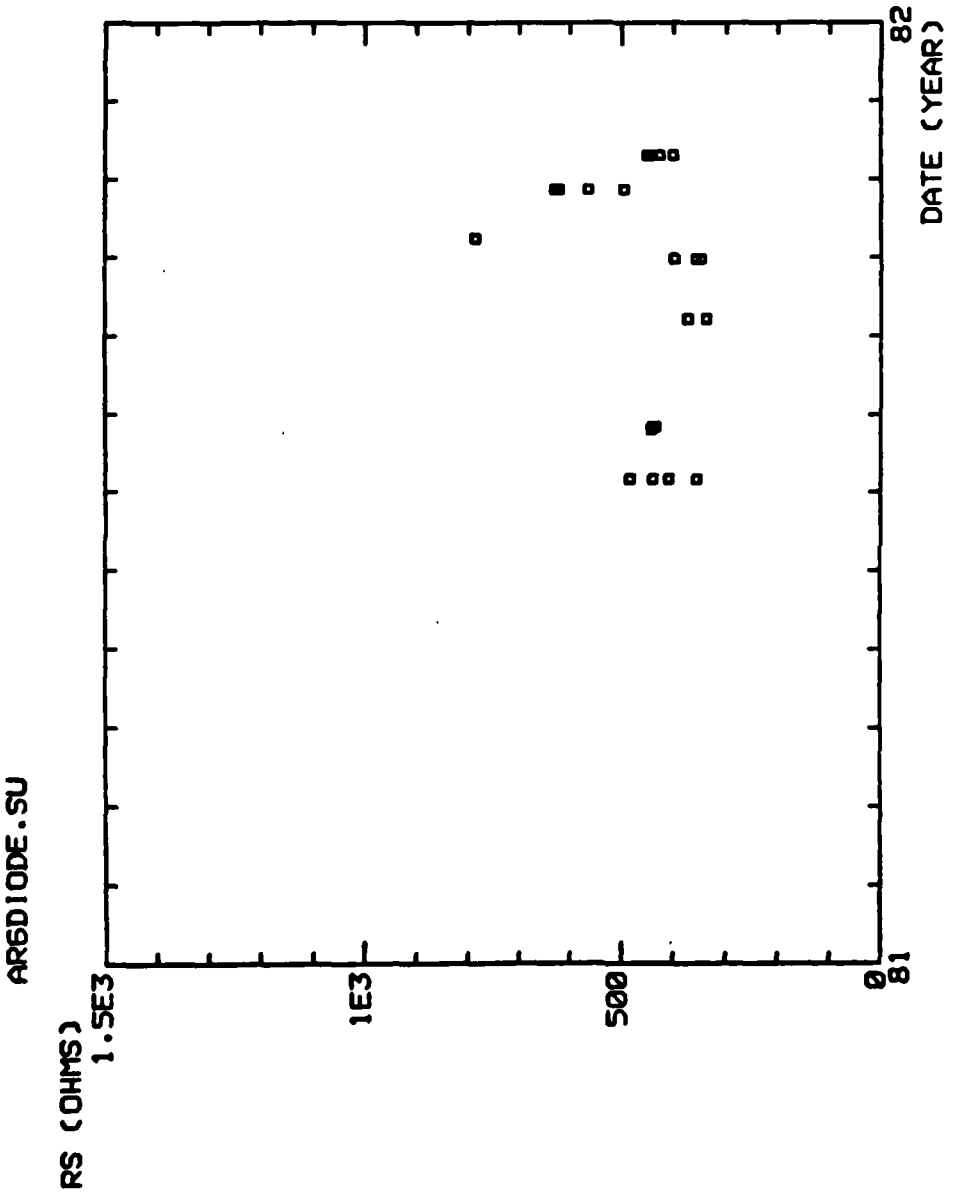


Fig. 4.4-5 History of logic diode series resistance, R_s, for the AR6 wafers. Each data point represents the mean for one wafer.

Table 4.4-1

Summary of Fabrication Results from AR6 Wafers

Number started	7 × 4 = 28
Number completed	25 (89%)
Number with required diode Rs range (<800Ω)	25 (89%)
Number with required V_p range (0.9V < V_p < 1.2 V)	20 (71%)
Number acceptable for circuit testing	20 (71%)

4.5 Reliability

One of the major factors for achieving good and reliable GaAs integrated circuits is to have a good Schottky and ohmic metallization system. Unlike Si integrated circuits where high quality polysilicon and metal silicides are easily formed, GaAs integrated circuits depend strictly on metals to form Schottky barriers or ohmic contacts. Although much work on various metallization systems has been done in the past, a clear understanding of the GaAs-metal interaction leading to standard fabrication recipes for the industry to follow has not been reached. Also, the reliability of the metallization systems and its impact on the device performance of GaAs ICs is not fully understood.

Metallization Reliabilty

The initial goals of the reliability work in this program were to establish the reliability of our devices and metal systems, to find out what the degradation mechanisms were, and to initiate corrective actions. Accelerated life test techniques with thermal stress have been initially used for this study.

As a starting point, characteristics of FETs and diodes after thermal aging were measured using our automatic probing system.[15] Table 4.5-1 shows the results obtained from one of our standard IC wafers which was cut into two halves with one section thermally aged at 240°C and the other section heated

at 150°C. Both heat treatments were done in air ambient. The characteristics of FETs and logic diodes were measured at different stages of the heat treatment using the standard T2 test patterns which are uniformly distributed on the wafers.[15] Each number on the table represents the mean values or standard deviations of the measured parameters for 36 devices. At 150°C no degradation was observed on the FETs even after 1000 hours of heat treatment. The average values of V_p, I_{dss}, and R_{on} remained nearly constant during this test. The series resistance of the diodes remained the same after 500 hours but increased slightly after 1000 hours. This is probably an indication of the onset of ohmic contact degradation. At 240°C the degradation of the FETs and the diodes can be clearly seen even after only few hours of heat treatment. It is interesting to note that although the current (I_{dss}) and the resistances (R_{on} and R_s) have degraded, the threshold voltage (V_p) remains stable. This suggests that the Ti/Au Schottky barrier is much more reliable than the ohmic contacts, and the major reason for the device degradation is deterioration of ohmic contacts.

Table 4.5-1
Characteristics of FETs (50 μm wide) and Diodes After Aging

MRDC81-11564

		BEFORE HEATING	240°C 2 HOURS	240°C 4 HOURS
FET	V_p (V)	1.036 ± .1	.9827±.102	1.009 ± .0984
	I_{DSS} (MA)	3.024 ± .411	2.469 ± .436	2.415 ± .445
	Ron (Ω)	204.9 ± 35	256.8 ± 48.5	276.7 ± 51.9
DIODE	Rs (Ω)	697.3 ± 105	1243 ± 398	1434 ± 481

		BEFORE HEATING	150°C 124 HOURS	150°C 336 HOURS	150°C 502 HOURS	150°C 983 HOURS
FET	Vp (V)	.9888 ± .0501	1.011 ± .0576	1.007 ± .0794	1.02 ± .0614	1.05 ± .0622
	I_{DSS} (MA)	2.991 ± .233	2.833 ± .386	2.908 ± .262	2.99 ± .263	3.088 ± .33
	Ron (Ω)	203.7 ± 31.9	209.8 ± 52.2	197.8 ± 20.2	190.8 ± 16	190.1 ± 18.1
DIODE	Rs (Ω)	676.8 ± 110	680.9 ± 105	701.9 ± 109	679.5 ± 107	732.9 ± 138

Ohmic contact reliability studies were conducted on test structures similar to the cross section of the metallization system for our standard FETs shown in Fig. 4.5-1. The ohmic contacts in the source and drain area consist of two layers of metals. The first layer is the alloyed ohmic metal, AuGe/Pt at the time when those experiments were conducted; the second layer is Ti/Au, which is the same metal used for the Schottky barrier gates.

In order to obtain direct measurement of the ohmic contact resistance an improved TLM test structure[14] which utilizes several ohmic gaps with different gap lengths was included in the AR5 mask set (designed and fabricated on a previous program).[1] This specific contact resistance structure was repeated so that a statistical sample size of 72 can be obtained from each wafer. The contact resistance of several wafers was monitored at frequent intervals during thermal aging tests, and these results were correlated with the device and circuit performance data.

The conclusion reached was that AuGe/Pt by itself forms excellent ohmic contact with GaAs, exhibited by low contact resistance and good morphology. Table 4.5-2 shows the specific contact resistance of AuGe/Pt contacts at different stages of aging at 250°C up to 300 hours. Little or no degradation was observed.

Table 4.5-2
Specific Contact Resistance (Ω-cm^2) of AuGe/Pt Ohmic Contacts
Without Schottky Overlay Heat Treated at 250°C

As Alloyed	2 Hours	10 Hours	50 Hours	150 Hours	300 Hours
4×10^{-6}	7.3×10^{-6}	7.7×10^{-6}	5.6×10^{-6}	4.6×10^{-6}	4.9×10^{-6}

The effect of varying the doping concentration (over a limited range) on the contact resistance was also studied. The dose of n^+ sulfur implant was varied over a range of sheet resistance from 250 $\Omega/\square$ up to 750 $\Omega/\square$. (Our typical sheet resistance is ~ 500 $\Omega/\square$). Table 4.5-3 shows the specific contact resistance and their reliability data corresponding to 4 different

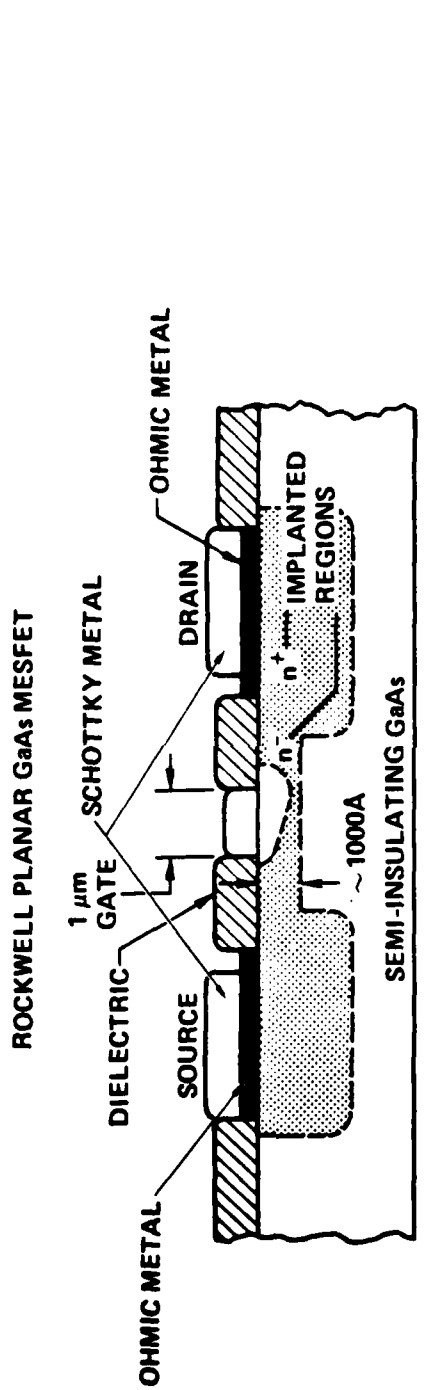


Fig. 4.5-1 Cross-section of the standard depletion mode GaAs MESFET used in SDFL logic.

doses. It is clear from the data that r_c is independent of the sheet resistance over this range and it is stable to 240°C.

It is important to note the reliability data of the ohmic contacts presented in Table 4.5-3 are obtained from AuGe/Pt contacts without Schottky metal overlay. When AuGe/Pt is covered by Schottky metal, a step necessary for circuit interconnection, the contacts start to degrade very rapidly. Fig. 4.5-2 shows the thermal aging behavior of the contact resistance for contacts with a Ti/Au overlay. In only several hours of aging at 240°C, the specific contact resistance increased from high 10^{-7} Ω-cm^2 to more than 10^{-5} Ω-cm^2. Device degradation is also apparent from the decrease in the average I_{dss} of 50 μm FETs and the increase in propagation delay time measured from ring oscillators. Several other Schottky overlay metals such as Ti/Pt/Au and TiW/Au were tested, but the thermal degradation results were similar indicating that Ti/Au overlay was not the problem, and the AuGe/Pt contact system itself had to be suspected.

Table 4.5-3
Thermal Reliability of AuGe/Pt Contacts* vs Sulfur Implant Dose

DOSE \ TIME	AS ALLOYED	240°C, 1 HR	4 HR	16 HR	64 HR
SULFUR 1.7×10^{13} cm^{-2}	$\bar{r}_c = 1.6 \times 10^{-6}$ Ω-cm^2 $\bar{\rho}_s = 263$ Ω/□	1.3×10^{-6} 261	1.2×10^{-6} 260	1.3×10^{-6} 260	1.3×10^{-6} 262
1.3×10^{13}	1.9×10^{-6} 309	1.4×10^{-6} 306	1.2×10^{-6} 307	1.3×10^{-6} 304	1.3×10^{-6} 308
➡ 9×10^{12}	1.4×10^{-6} 493	1.2×10^{-6} 492	0.9×10^{-6} 508	1.1×10^{-6} 508	1.2×10^{-6} 504
5×10^{12}	2.1×10^{-6} 753	1.4×10^{-6} 754	1.2×10^{-6} 762	1.7×10^{-6} 740	1.8×10^{-6} 753

*NO OVERLAY METAL

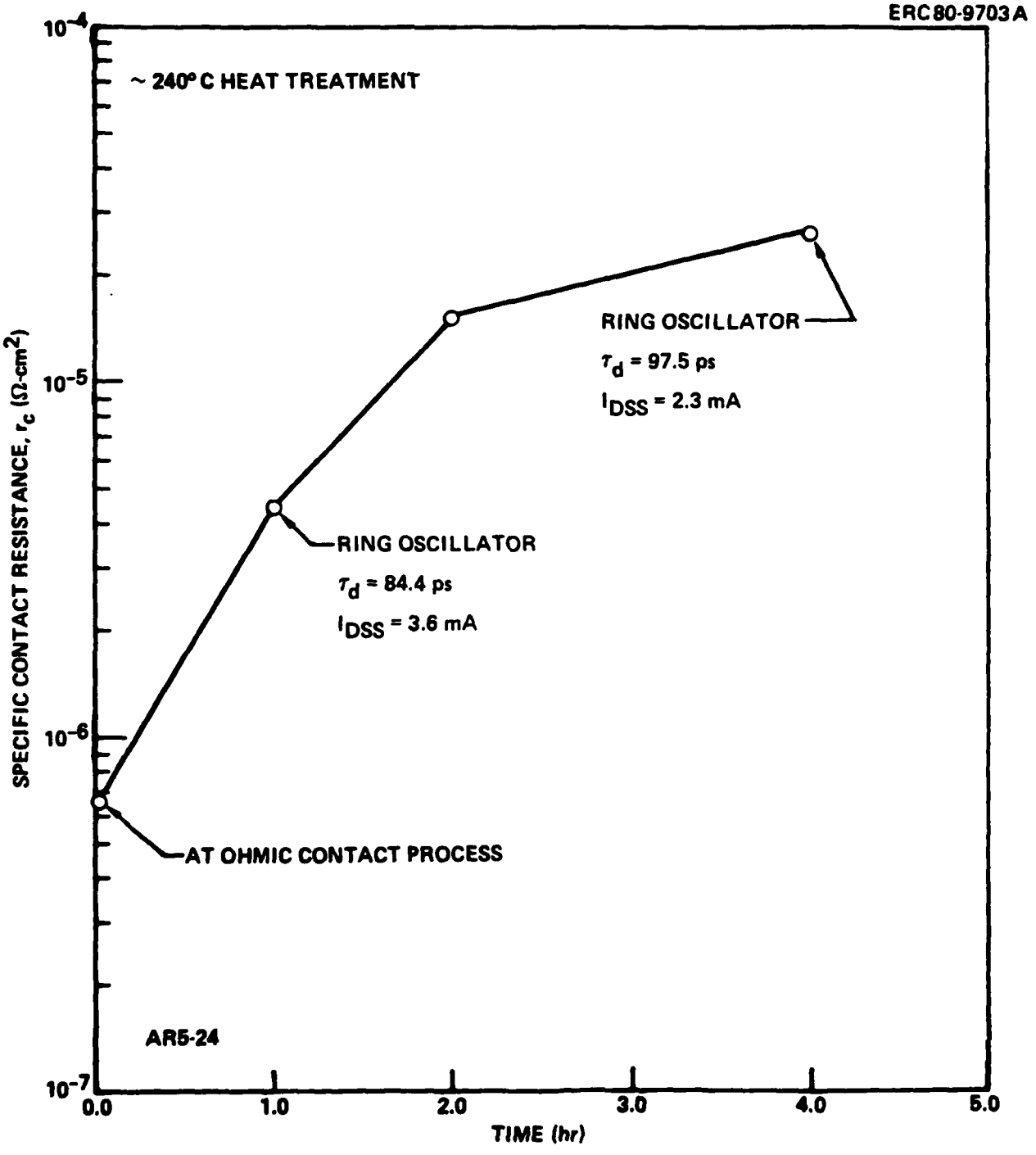


Fig. 4.5-2 Reliability of AuGe/Pt ohmic contacts with Schottky metal overlay.

As mentioned earlier, the Schottky metal in our process is more reliable than the ohmic contacts. In order to observe degradation, higher thermal aging temperatures were required. Samples with various Schottky metals were aged at several different temperatures and different time intervals. The Schottky barriers were characterized by I-V measurements; the ideality factor (n) and the Schottky barrier height (ϕ_B) were determined using the thermionic-emission model. Table 4.5-4 shows a comparison between Au, Pt/Au, Ti/Au and Ti/Pt/Au. Above 400°C all of these metal systems started to degrade. The degradation of Au is evident even at 320°C. The other three retained good diode characteristics at 320°C for two hours of aging. However, the barrier height of Pt/Au decreased, and the barrier height of Ti/Au increased.

This behavior can be explained by the diffusion of Au through the thin Pt and Ti layers. As Au reaches the GaAs surface the Schottky barriers no longer behave like Ti or Pt barriers but like Au barriers, Au having a barrier higher than Ti and lower than Pt. The data indicate that the Ti/Pt/Au Schottky barrier is more stable than Ti/Au and Pt/Au when heat treated at 320°C. Since the Pt layer is sandwiched between Au and Ti, it acts as an Au diffusion barrier preventing Au from reaching the GaAs surface. In order to study the effectiveness

Table 4.5-4

Comparison of Schottky Barriers Between Au, Pt/Au, Ti/Au and Ti/Pt/Au

ERC80-9715

SCHOTTKY METAL	AS DEPOSITED	320°C 2 HRS	400°C 2 HRS	500°C 2 HRS
Au 1500Å	η = 1.01 ϕ_B = 0.873 eV	1.21 0.882	1.18 0.888	BAD DIODE
Pt/Au 300/1000Å	1.03 0.962	1.06 0.908	2.18 0.75	BAD DIODE
Ti/Au 300/1000Å	1.02 0.777	1.04 0.878	1.2 0.796	BAD DIODE
Ti/Pt/Au 300/300/1000Å	1.032 0.775	1.033 0.776	SCATTERED DATA	BAD DIODE

η (IDEALITY FACTOR)
ϕ_B (BARRIER HEIGHT)

of the Pt barrier, Ti/Pt/Au Schottky diodes were fabricated with different thicknesses of Pt and aged at 240°C and 320°C. The electrical results are shown in Table 4.5-5. The thicker the Pt layer is, the more stable the barrier height, although the difference is not very significant. However when the Pt layer is thicker, the Schottky metal processing step is more difficult because of the stress induced by the high density Pt film and the heat generated during evaporation. Based on these experiments, Ti/Pt/Au with thicknesses of 300Å/300Å/ 2400Å was incorporated into our GaAs IC process replacing the simple Ti/Au used previously.

As indicated above, the primary factor limiting circuit reliability was the thermal stability of the ohmic contacts. AuGe/Pt, the ohmic metal which had been used in the past, was not reliable when thermally treated at high temperatures (> 200°C). Although this metal system provides smooth surface morphology

Table 4.5-5

The Effect of the Pt Layer on the Reliability of Ti/Pt/Au Schottky Barriers

ERC80-9714

SCHOTTKY METAL	AS DEPOSITED	240°C 25 HR	240°C 125 HR	320°C 2 HR	320°C 8 HR
Ti/Au 300/2700Å	η = 1.07 ϕ_B = 0.774	1.06 0.811	1.174 0.844	1.12 0.856	1.4 0.787
Ti/Pt/Au 300/300/2400Å	1.03 0.762	1.06 0.79	1.05 0.793	1.07 0.799	1.06 0.813
Ti/Pt/Au 300/600/2100Å	1.05 0.777	1.07 0.78	1.04 0.787	1.08 0.79	1.15 0.78
Ti/Pt/Au 300/900/1800Å	1.06 0.744	1.06 0.785	1.12 0.781	1.09 0.782	1.06 0.794

η (IDEALITY FACTOR)
ϕ_B (BARRIER HEIGHT)

and low contact resistance after alloying, it degrades rapidly when thermally aged.

To improve the reliability of the ohmic contacts, another metal system, AuGe/Ni, was studied, and its thermal reliability was evaluated. It was found that this metal system was much more stable than AuGe/Pt. In order to have a good comparison between these two systems, wafers were processed with AuGe/Pt on one half and AuGe/Ni on the other half of the same wafer. All the processing steps including the alloying cycle were the same for both metals. The wafers were aged at 240°C in air ambient for reliability testing. Specific contact resistance, device characteristics and circuit performance were evaluated before and after aging.

In the following discussions the results from one of the wafers, AR5-82 are used as an example. Half of the wafer has AuGe/Pt contacts. The specific contact resistance (r_c) was determined by TLM (transmission line model) method using the T1 test pattern, which is uniformly distributed on the wafer.[15] Table 4.5-6 shows the measured r_c values at different stages of processing and after thermal aging (at 240°C). After the Schottky metallization, the specific contact resistance of AuGe/Pt was already much higher than that of AuGe/Ni. The AuGe/Ni contact continued to degrade with further processing and thermal aging. The degradation during the second level metal processing step is probably due to the heating cycle used during the deposition of plasma silicon nitride. The r_c for AuGe/Pt after Schottky metallization is higher than the typical r_c (in the 10^{-6} Ω-cm^2 range) of AuGe/Pt immediately after alloying. This indicates that the degradation had already occurred during the Schottky metallization step. Degradation is probably due to the thermal treatment involved in the processing and/or the influence of the Schottky metal overlay. AuGe/Ni, on the other hand, had a very low initial r_c value ($< 10^{-6}$ Ω-cm^2) and showed excellent thermal stability during process and during thermal aging.

Table 4.5-6

Comparison of AuGe/Pt and AuGe/Ni Ohmic Contacts

	Specific Contact Resistance (Ω-cm^2)	
	AuGe/Pt	AuGe/Ni
After Schottky metal process	$2.45 \pm 1.55 \times 10^{-5}$	$7.58 \pm 5.71 \times 10^{-7}$
After 2nd level metal process	$1.56 \pm 1.1 \times 10^{-4}$	$7.6 \pm 6.6 \times 10^{-7}$
After 2.5 hours aging (240°C)	$1.93 \pm 1.21 \times 10^{-4}$	$9.08 \pm 7.77 \times 10^{-7}$
After 22 hours aging (240°C)	$3.31 \pm 2.05 \times 10^{-4}$	$9.6 \pm 9.36 \times 10^{-7}$

Because the sizes of the FETs and diodes in the GaAs ICs are very small, the contact resistance has a strong influence on device characteristics. Bad ohmic contacts usually result in high diode series resistance (R_s) and low FET saturation current (I_{dss}). Our automatic probing system was used to measure the characteristics of the 50 μm wide, 1 μm gate FETs and the 1 × 2 μm diodes in the T2 test cell[15] on the wafer before and after aging. As shown in Table 4.5-7 the diodes with AuGe/Ni ohmic contact had low series resistance, and the resistance stayed low after aging. The diodes with AuGe/Pt ohmic contact, had higher initial series resistance, and the resistance increased with aging. Similar effect was found for I_{dss} of the FETs, I_{dss} stayed almost unchanged with AuGe/Ni contacts, and it degraded with AuGe/Pt contacts (Table 4.5-7). The change in I_{dss}, due to the negative feedback effect of the source series resistance, is seen very clearly in the scatter plots of I_{dss} versus V_p shown in Fig. 4.5-3.

Table 4.5-7

Series Resistance of 1 μm × 2 μm Diodes and I_{dss} of 50 μm FETs Before and After Aging. The Data Represents Wafer Mean and Standard Deviation

	Diode Series Resistance (Ω)			
	After SM Process	After 2M Process	2.5 Hours at 240°C	22 Hours at 240°C
AuGe/Ni	309.8 ± 72.9	309.7 ± 70.2	329.3 ± 77	317.3 ± 76
AuGe/Pt	434.5 ± 87	668 ± 175.7	688.7 ± 149.5	844 ± 222
		I_{dss} (mA)		
AuGe/Ni	4.05 ± 0.367	3.99 ± 0.43	3.967 ± 0.42	4.022 ± 0.417
AuGe/Pt	3.678 ± 0.37	3 ± 0.344	2.872 ± 0.35	2.594 ± 0.316

Each point in the plots represents one of the 72 test FETs over the wafer. Note that one half were processed with AuGe/Pt and the other half with AuGe/Ni. After the Schottky metal process (Fig. 4.5-3a) the existence of two groups of points is barely noticeable. No clear distinction can be made between FETs with AuGe/Pt contacts and FETs with AuGe/Ni contacts. However, after the second level metal process, two families of FETs are clearly seen on Fig. 4.5-3b. Although they have similar threshold voltages, the currents are different. The devices with higher currents have AuGe/Ni contacts and the one with lower current have AuGe/Pt contacts. With further aging (Figs. 4.5-3c and 4.5-3d) the separation between these two families becomes wider and wider, indicating further degradation of the AuGe/Pt contacts.

The effect of the ohmic contact resistance on circuit performance was studied using the 9-stage 10 μm (FET width) NOR gate ring oscillators on the 4 PM (drop-in) chips of the wafers.[15] Two of the drop-ins have AuGe/Pt contacts, and the other two have AuGe/Ni contacts. They were tested before and after aging with fixed bias (V_{DD} = 2V, V_{SS} = -1V) and with bias optimized for operation at the highest frequency. The circuit performance data are summarized in Table 4.5-8. The results show clear difference in performance for ring oscillators with AuGe/Pt contacts and with AuGe/Ni contacts. The ones

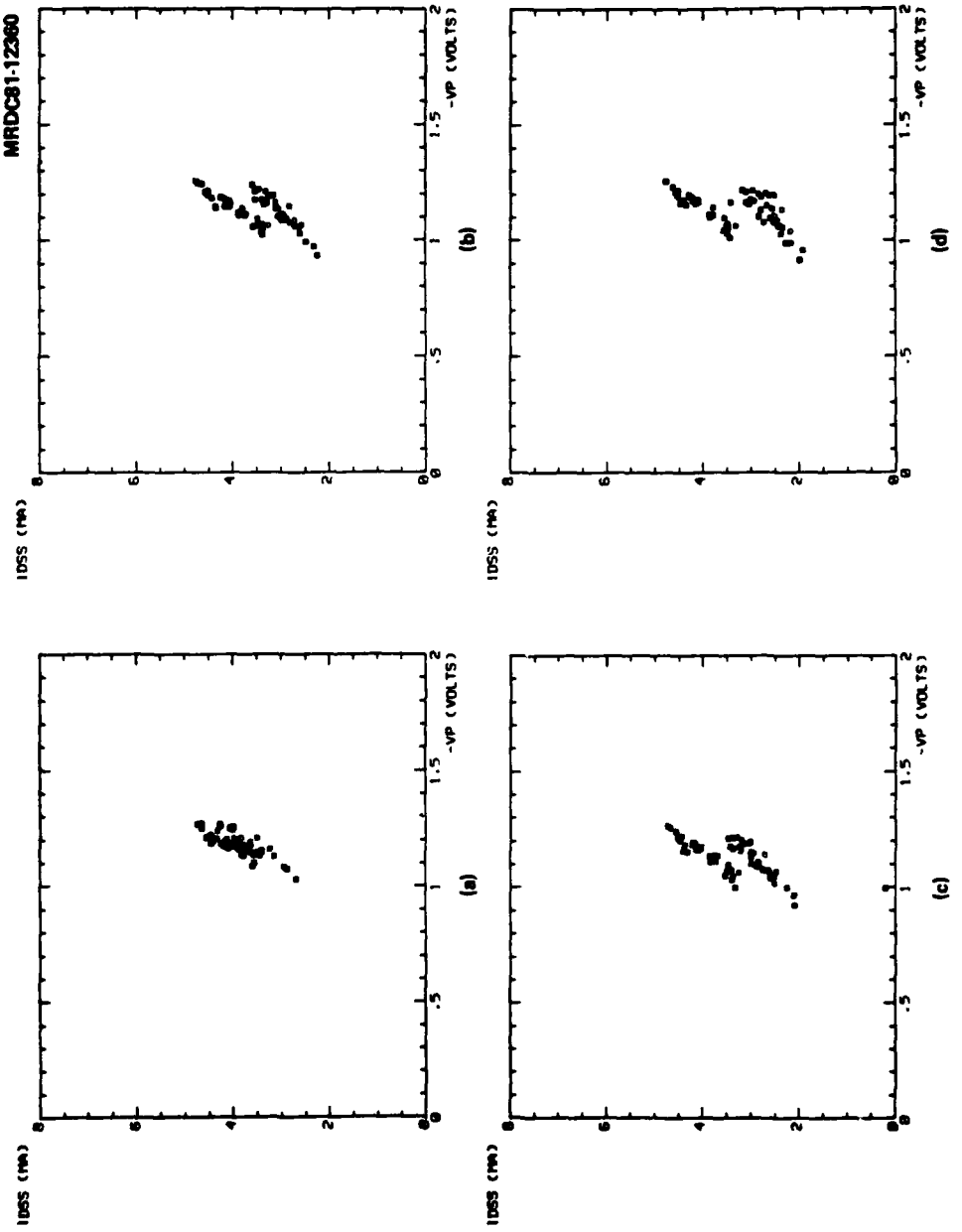


Fig. 4.5-3 I_{dss} vs V_p for all the 72 test FETs on a wafer at different stages of process and thermal treatment. a) After Schottky metalization; b) after second layer metalization; c) after aging for 2.5 hrs at 240°C, and d) after aging for 22 hrs at 240°C.

with AuGe/Ni contacts oscillate faster and have lower speed-power product than those with AuGe/Pt contacts. After aging for 22 hours at 240°C, the ring oscillators with AuGe/Pt contacts degraded; the propagation delay time increased about 30 ps/gate. The ring oscillators with AuGe/Ni contacts maintained good speed after aging. No significant change in circuit performance was observed. The best result obtained on this wafer showed a propagation delay τ_D = 71 ps/gate and a speed-power product $P_d\tau_D$ = 52 fJ. The circuit performance data presented above agree with the specific contact resistance data shown on Table 4.5-6 and the device data shown on Table 4.5-7.

Having recognized the difference in reliability between AuGe/Pt contacts and AuGe/Ni contacts, the standard ohmic metallization system was changed from AuGe/Pt to AuGe/Ni. This change resulted in significant improvement in contact resistance. Figure 4.5-4 shows the history of the contact resistance (R_c) and specific contact resistance (r_c) over a relatively long period of time. These data were obtained through the routine process evaluation measurements taken with our automatic test facility.[15] Each point in the graph represents the mean value of R_c or r_c on a wafer. A transition at the end of 1980 resulting in lower contact resistance as a consequence of replacing AuGe/Pt by AuGe/Ni is clearly seen in the figure.

Circuit Reliability

The investigation of the reliability of GaAs integrated circuits is more complex than that of discrete MESFETs. The complexity is due to the use of more complex metallization systems, the need to maintain isolation between devices, the large number of transistors and diodes on a chip, the complexity of the dielectric systems, the length of interconnections, and the existence of large numbers of crossovers. Preliminary work was done by high temperature storage tests on 9-stage ring oscillators. The data showed an activation energy of 1.41 eV for degradation, and a lifetime of more than 10^{13} hours at room temperature was predicted. These figures are comparable to those that have been reported for discrete GaAs MESFETs.

Table 4.5-8

Ring Oscillator Performance Before and After Aging

Device No.	V_{DD}(V)	I_{DD}(mA)	V_{SS}	I_{SS}	f(MHz)	P(mW)	τ(PS)	Pτ(fJ)	
				Before Aging					
1	2	2.47	1	0.84	410	0.578	135.5	78.3	AuGe/Pt
2	2	2.4	1	0.92	470	0.572	118.2	67.6	
3	2	2.82	1	0.9	540	0.654	102.9	67.3	AuGe/Ni
4	2	3.47	1	1.05	630	0.799	88.2	70.4	
				Bias Condition Optimized for Highest Frequency Operation					
1	2.069	2.82	0.694	0.7	460	0.632	120.8	76.3	AuGe/Pt
2	2.02	2.7	0.73	0.8	530	0.604	104.8	63.3	
3	1.616	2.83	0.768	0.9	690	0.526	80.5	42.4	AuGe/Ni
4	1.714	3.94	0.702	0.93	782	0.74	71	52.6	
				After Aging at 240°C for 22 Hours					
1	2	2.07	1	0.7	293	0.484	189.6	91.7	AuGe/Pt
2	2	2.2	1	0.68	390	0.508	142.4	72.3	
3	2	2.62	1	0.86	538	0.61	103.3	63	AuGe/Ni
4	2	3.4	1	1	626	0.78	88.7	69.2	
				Bias Condition Optimized for Highest Frequency Operation					
1	2.081	2.42	0.669	0.61	362	0.544	153.5	83.5	AuGe/Pt
2	1.833	2.35	0.757	0.57	418	0.474	132.9	63	
3	1.575	2.79	0.708	0.78	695	0.495	79.9	39.5	AuGe/Ni
4	1.705	3.85	0.68	0.9	780	0.717	71.2	51.1	

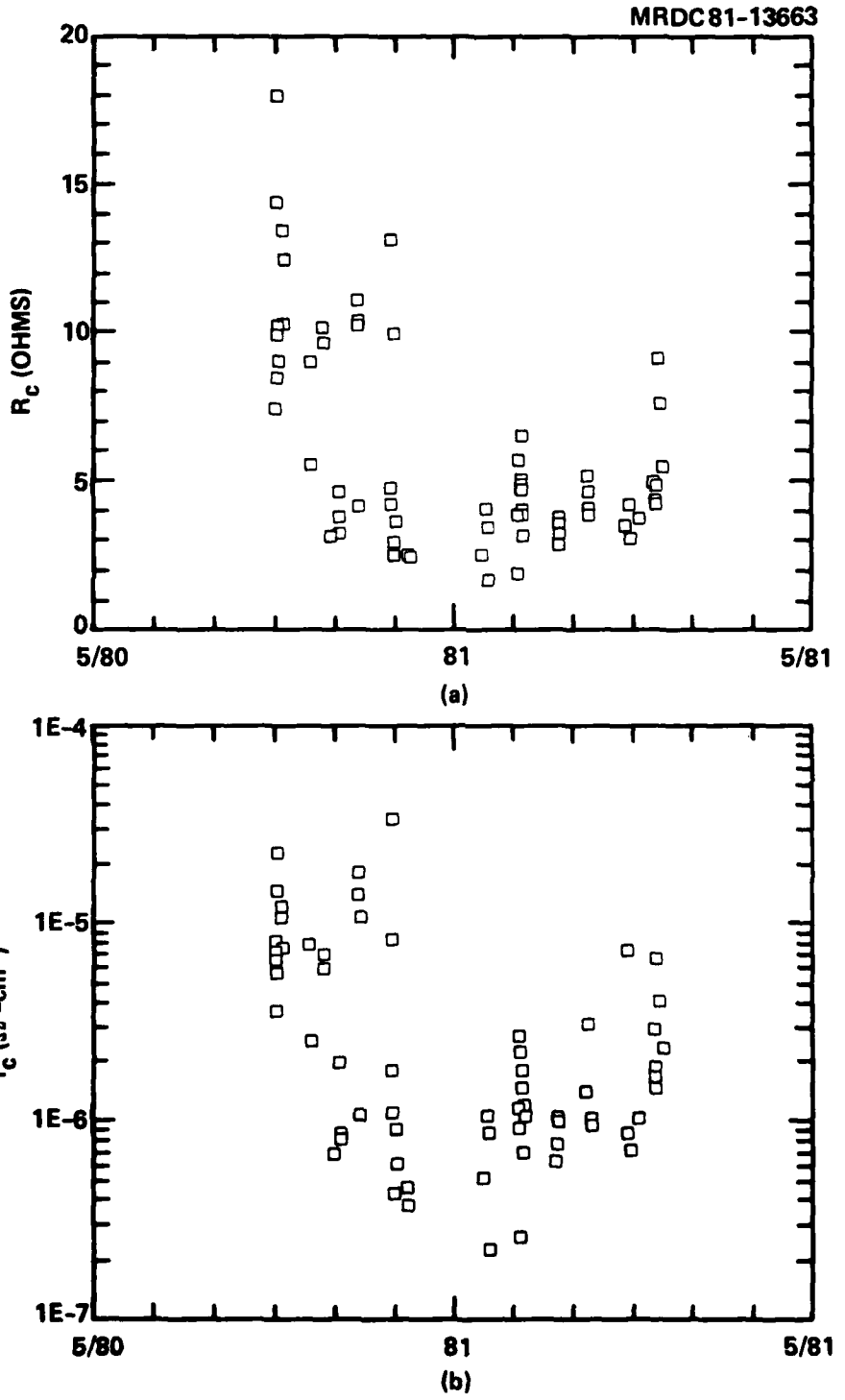


Fig. 4.5-4 History of ohmic contact resistance over a 12 month period. Each data point corresponds to the mean for one wafer of a) total contact resistance; b) specific contact resistance.

Further reliability studies have been carried out on circuits under bias. Ring oscillators with 9 inverter stages were chosen for this study. Each stage in the circuits contained a 10μm wide switching FET, an 8μm wide pull-up active load, and a 2μm wide pull-down transistor, all with a gate length of 1μm. The circuits were packaged into 24-pin flat-packs, which could accommodate six devices in each package, and were suitable for high-frequency operation. The packages were mounted in a test fixture in which the flat-pack leads were pressed using O-ring material onto two ceramic substrates. The substrates were separated by the width of the flat-pack. The substrates had a gold line patterned designed to match the package leads, and such that the lines had 50-ohm characteristic impedance. The substrates were placed in a copper outer shell on which the SMA connectors and dc feedthroughs were mounted to connect the metal lines on the substrates to the outside wiring. The coaxial cables and the wires used were chosen to have Teflon coating so that they could be used at high temperatures. A bench-top forced-air convection oven was used to provide the high temperature environment.

The power supply biases were applied to the circuits through a switch box in which each line was connected in series with a low power fuse so that the shorting of one device would not affect other devices. The readings of the supply current values and the frequency of oscillation of each device could be selected by the switch box. The oscillation frequency was measured with a spectrum analyzer.

Two temperatures, 200°C and 250°C, were selected for high temperature testing; the tests were carried out in flowing N_2 ambient. From room temperature to high temperatures, the current values, I_{dd} and I_{ss}, of the devices increased, and the oscillation frequency decreased. The increase of the currents is explained by built-in potential changes at the Schottky gate and the channel-substrate interface of the FETs, and the decrease of the frequency is presumably due to the lower electron mobility at high temperatures. When the devices reached the testing temperature, the operations of the devices stabilized, and the degradation with time was very slow. At 200°C, five devices were tested for a period of more than 400 hours. The normalized values of the oscillation frequencies of the circuits as functions of aging time are shown

in Fig. 4.5-5. Four devices were started at 250°C, but one ceased operation after 70 hours due to instrumentation problems, not device failure. The other three were tested for about 400 hours. The oscillation frequencies are plotted against aging time in Fig. 4.5-6. The devices degraded at a faster rate than those aged at 200°C, but most of the degradation occurred during the first 150 hours of operation. After that time the devices stabilized and degraded at very slow rate.

For estimating the lifetime of the devices, the failure of a ring oscillator was arbitrarily defined as the point when the frequency of oscillation at the given temperature reaches a 20% degradation. At 200°C, a median life of 3700 hours was estimated from Fig. 4.5-5. At 250°C, because of the nonlinear relation between the oscillation frequency and the aging time, a worst case median life was estimated by using the data from the first 150 hours of operation. In this way a median life of 35 hours was obtained. By plotting the median life against the inverse of temperature in a semi-log form, and joining the two data points with a straight line, as shown in Fig. 4.5-7, an activation energy of 0.98 eV was obtained. If the straight line is extrapolated to room temperature an estimated lifetime of more than 10^9 hours is obtained.

It should be noted that the extrapolation technique used above is valid only for gradual (or slow) degradation; catastrophic failures are not included. No such failure was observed in 400 hours of aging at 200°C and 250°C for the small population tested. Although these results are very promising, a larger sample population needs to be tested, and more temperature data points need to be obtained.

4.6 Setup of 3-inch Diameter GaAs Wafer Processing

It is indispensable for the attainment of GaAs LSI/VLSI capability to fabricate integrated circuits on large diameter wafers. Based on this consideration, a decision was made to make a transition from the present processing 1 inch square GaAs wafer to the processing of 3 inch diameter circular wafers. It would have been extremely impractical and probably impossible to make this change with the limitations imposed by the Canon 4X projection aligner which

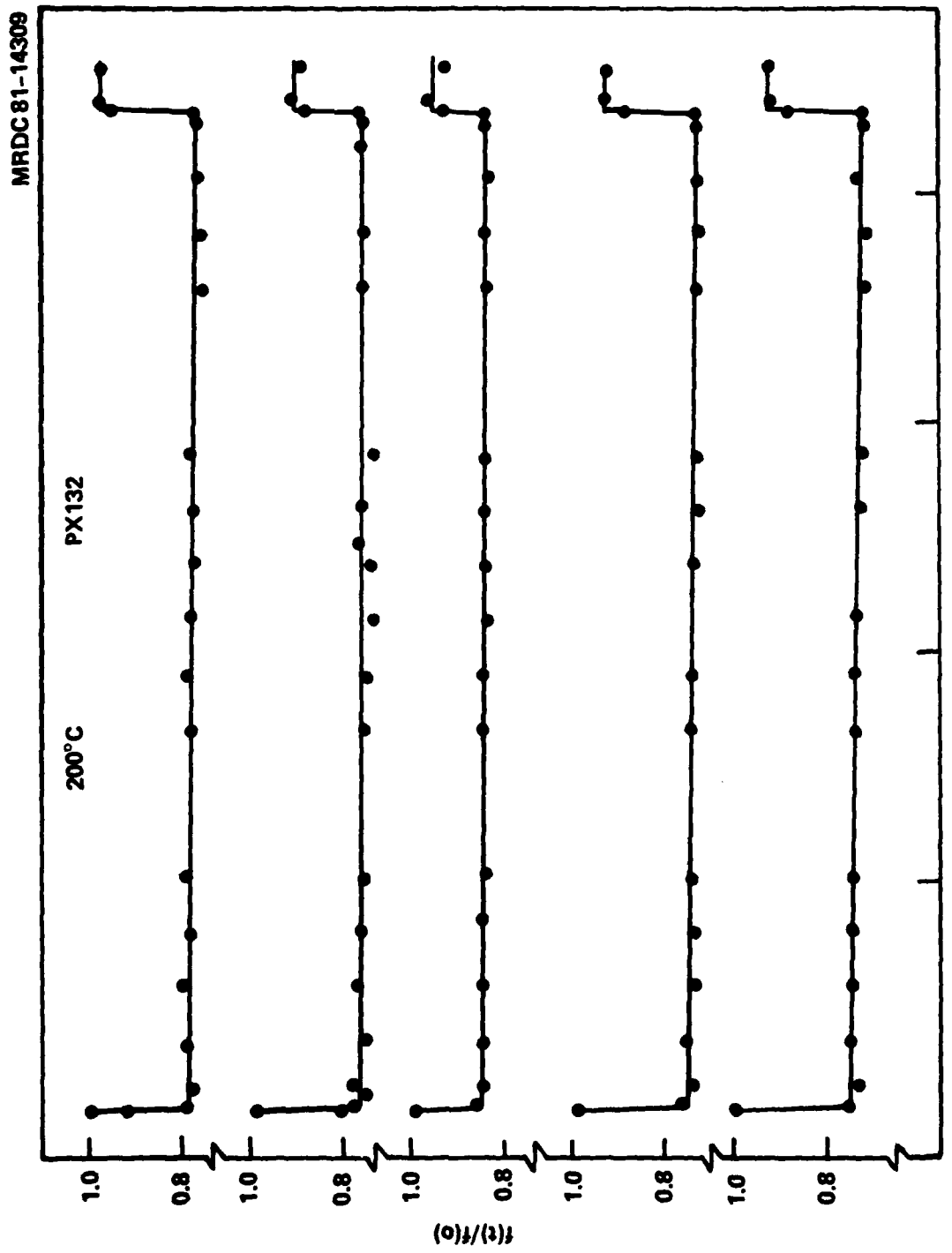


Fig. 4.5-5 Oscillation frequency vs aging time for five 9-stage ring oscillators operating at 200°C. The frequencies are normalized to the room temperature frequence at t = 0.

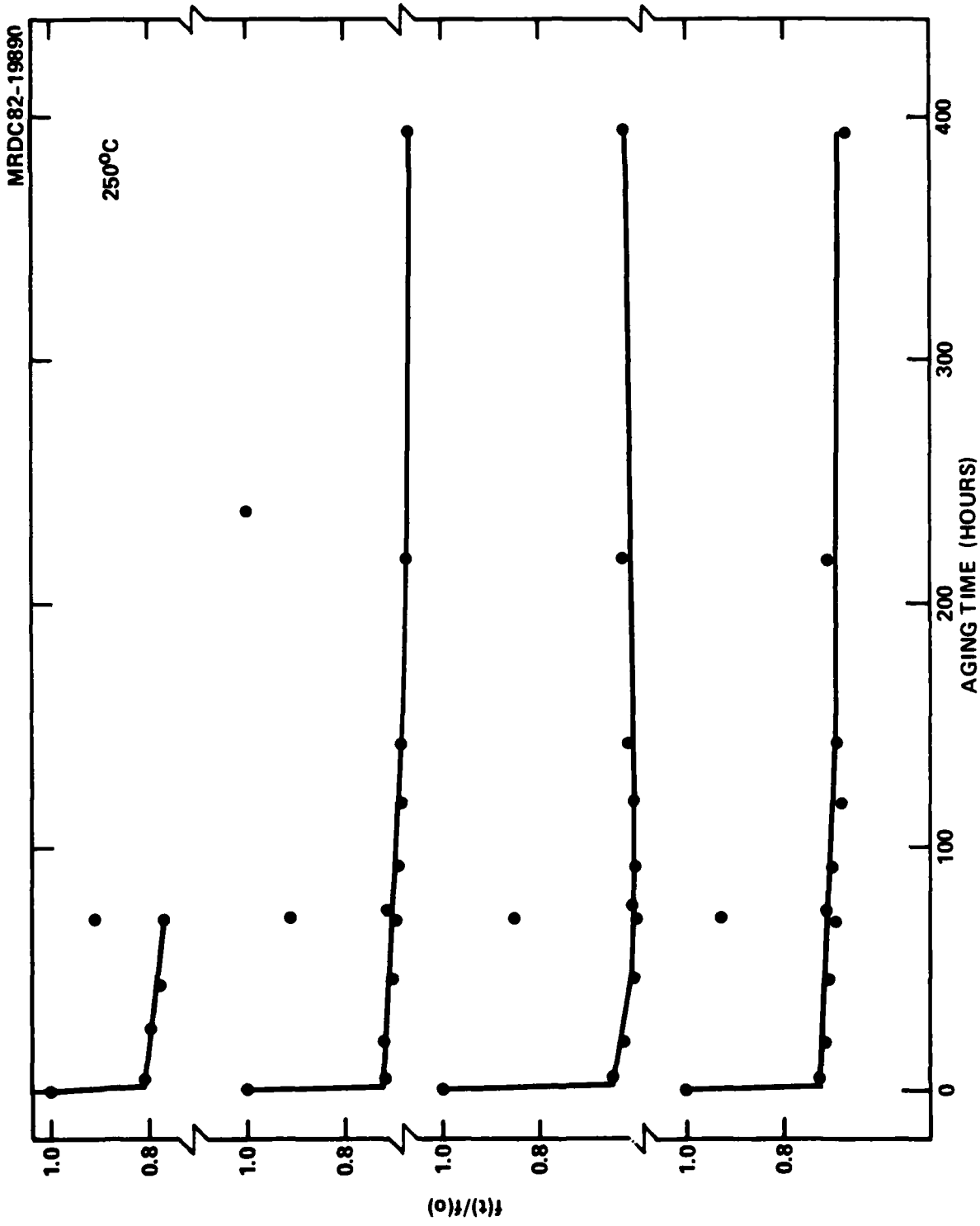


Fig. 4.5-6 Oscillation frequency vs aging time for five 9-stage ring oscillators operating at 250°C. The frequencies are normalized to the room temperature frequence at t = 0. The failure of one device was due to an instrumentation problem.

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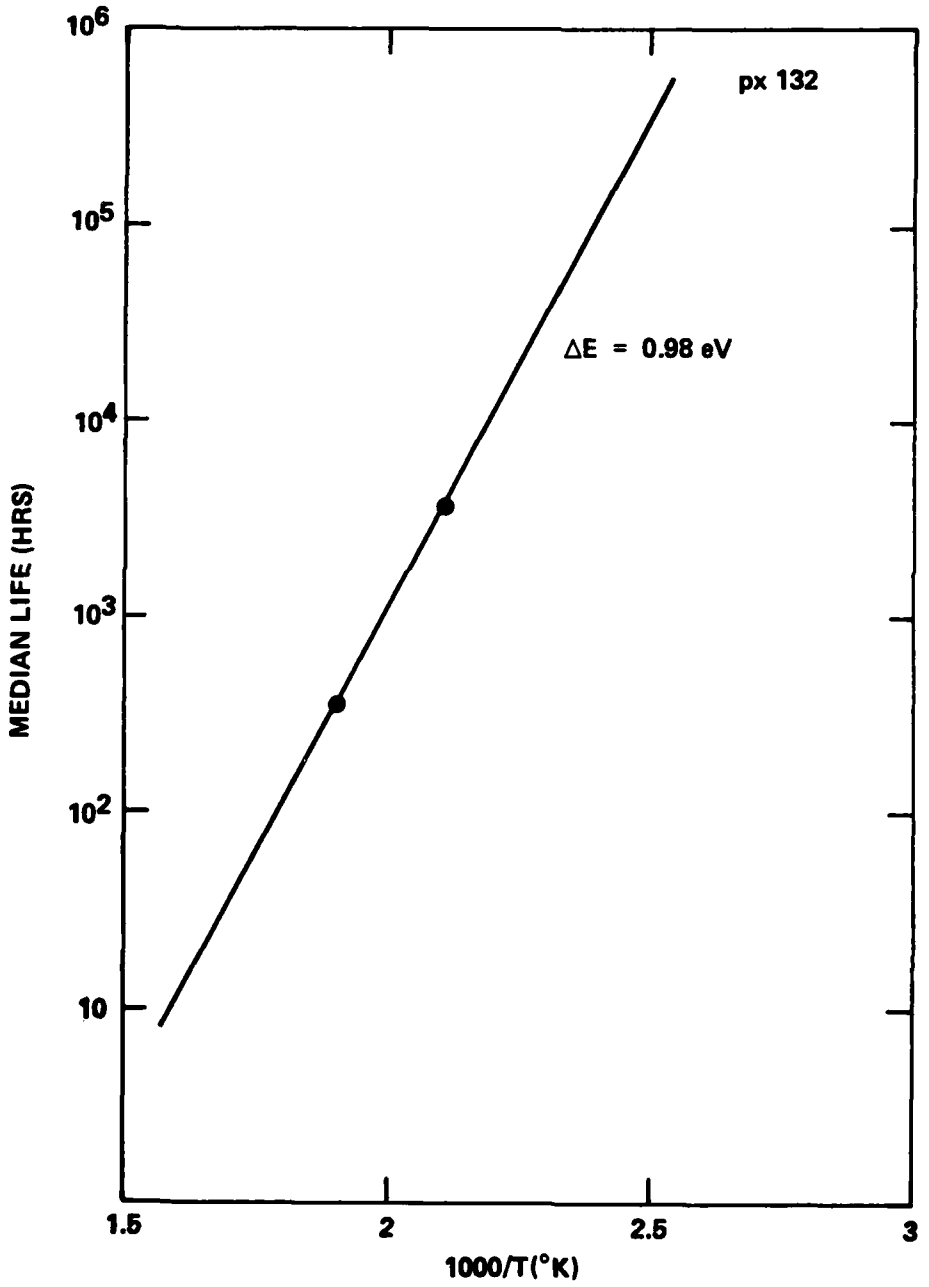

Fig. 4.5-7 Arrhenius plot for the medium lifetime of 9-stage ring oscillators. Failure was defined as the point when the oscillation frequency at the given temperature degrades by 20%.

has been used in all the GaAs digital IC projects at our facility. Consequently, a direct step on wafer (DSW) system was selected and acquired. A Censor SRA-100 10X projection aligner was chosen. Figure 4.6-1 shows a photograph of the system. This system is equipped to handle both 1 inch square wafers and 3 inch diameter circular wafers, thereby allowing an easy photolithography processing transition to take place.

The Censor DSW was selected because it had the best specifications and it contained certain features not available on any other equipment. The specifications of this system are: better than 1 μm resolution; automatic X, Y and θ field by field alignment with ±0.1 μm (1σ) overlay precision; automatic focusing; and field by field automatic leveling. This last feature, field by field leveling, was unique to this system and is particularly important since the Censor high resolution Zeiss lens has a small depth of focus (±1.5 μm) by virtue of its high (0.35 na) numerical aperture. In practice, this local field-by-field leveling feature eases the flatness specification of the GaAs wafers, and allows the submicron resolution capability of the lens system to be utilized effectively.

This Censor DSW equipment can provide repeatable and precisely controlled photolighographic processing. For example, Fig. 4.6-2 shows the histograms of alignment vernier readings (X_{Top}, X_{Bottom}, Y) from 10 wafers randomly selected for an alignment test. These statistical results confirm that this equipment is capable of an overlay accuracy of mean +3σ of < 0.25 μm.

Besides the excellent overlay results, resolution patterns surveyed during the same tests showed resolution consistently lower than or equal to 1 μm. The majority (> 50%) of the patterns exhibited ~ 0.875 μm resolution on all the wafers surveyed. Figure 4.6-3 illustrates the distribution of patterns resolved as measured from 13 three-inch wafers (416 fields).

The preliminary lithography tests discussed above had been performed using unprocessed (flat topology) wafers with optimal resist patterns for the overlay tests. Thus, the first requirement for actual wafer lots was to define and fabricate alignment marks. These marks must provide maximum edge

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Fig. 4.6-1 Photograph of the Censor SRA-100 DSW system.

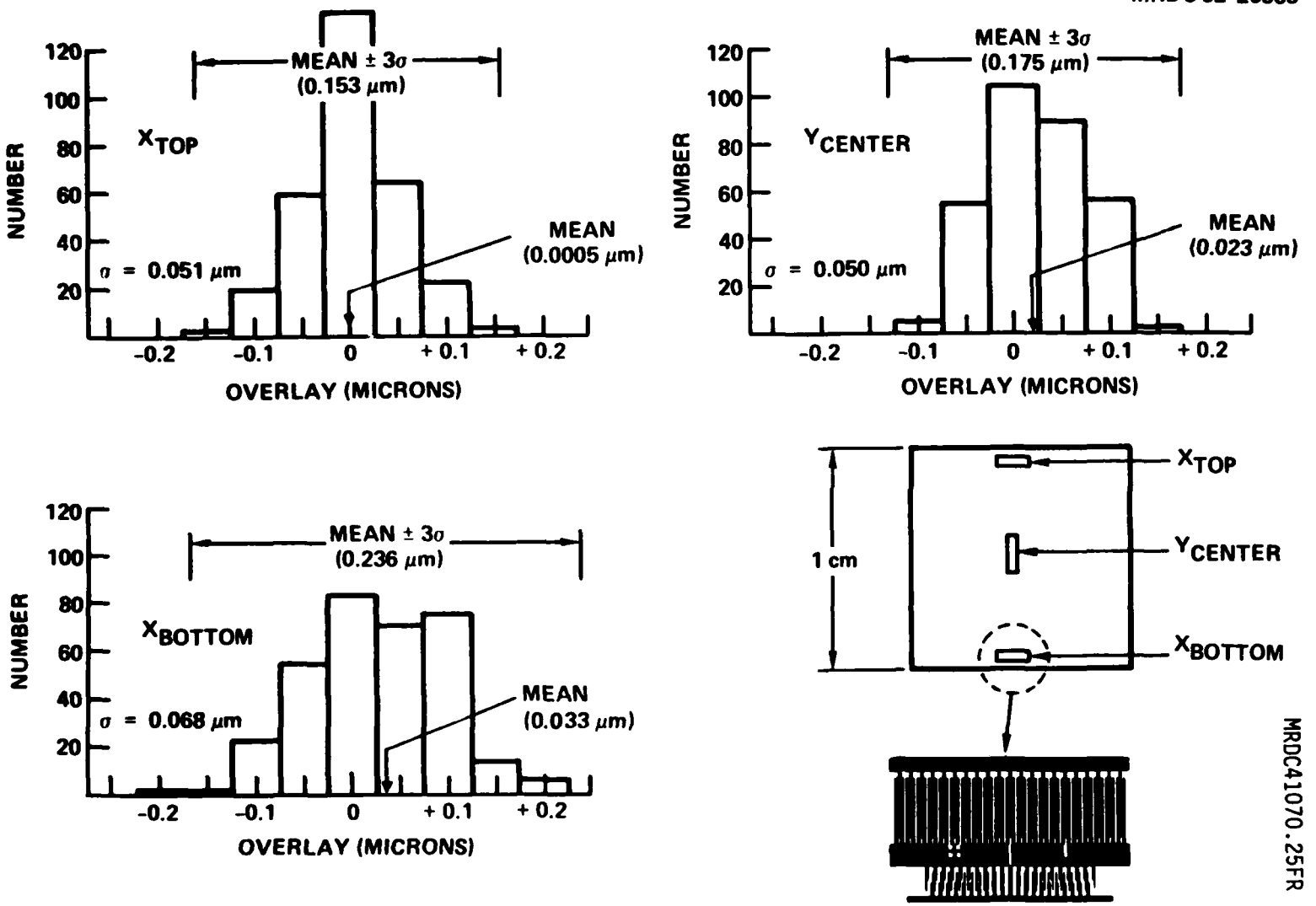

Fig. 4.6-2 Characterization of the alignment accuracy of the Censor projection aligner.

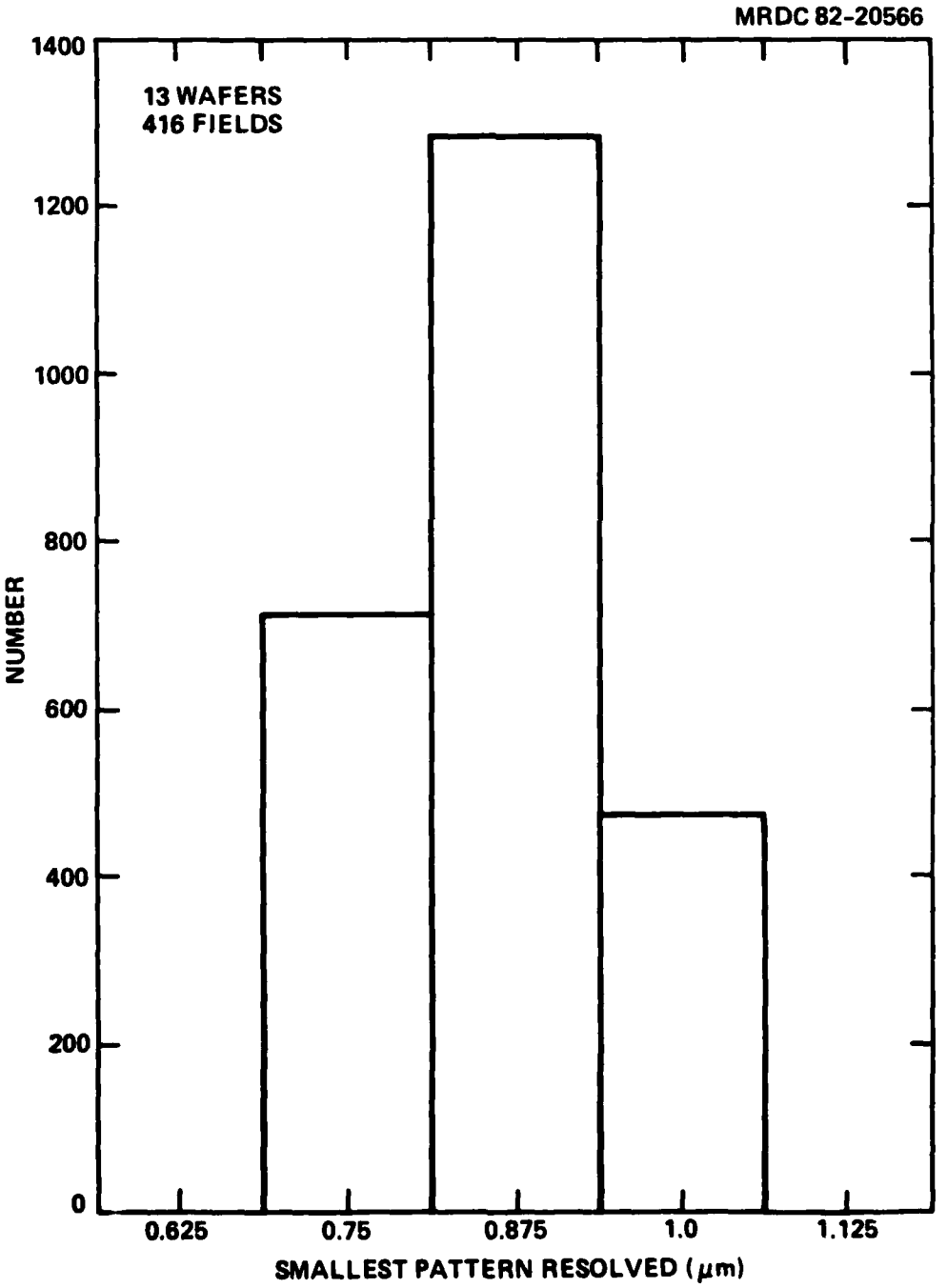

Fig. 4.6-3 Censor SRA-100 resolution test results.

acuity as well as maximum contrast in order to obtain the best possible overlay precision. After investigating several alignment schemes, titanium metal embedded between the Si_3N_4 and SiO_2 layers was chosen as a high yield, high contact technique. The titanium metal, while maintaining good reflectivity throughout the process, was also able to withstand the 850°C port implant anneal. All process steps up to and including the Schottky metal level use the same alignment marks, and thus level-to-level registration should be excellent.

As an additional test of resolution capability consistent with actual wafer processing, a critical dimension experiment was carried out. By measuring the resistance of long metal lines after etching and lift-off, and plotting the results with respect to known mask dimensions, a measure of linewidth control under actual processing conditions could be obtained. Figure 4.6-4 shows a plot of the length/resistance ratio as a function of various linewidths on the mask. By extrapolation to zero linelength, a measure of the replicated error could be determined. Figure 4.6-5 shows the critical dimension control statistics for the nominal 1.0 μm measurement made on three wafers. These results are very good, and demonstrate the current capabilities of the DSW plasma etched lift-off process.

Dry etching techniques, such as the reactive ion etching of SiO_2 layers, are of primary importance. A key element in this process is to significantly reduce the erosion of photoresist and Si_3N_4 while still maintaining a reasonable SiO_2 etch rate. The use of CHF_3 plasmas was found to be beneficial in this regard; however, the large hydrogen fraction tended to form a polymer layer on the etched surfaces. The use of CF_4 and H_2 gas mixtures was pursued and found to be a much more practical and controllable technique for etching. As shown in Fig. 4.6-6, the continued addition of H_2 tends to suppress photoresist erosion while maintaining a high SiO_2 etch rate. The point of polymer formation was determined to ≈40% H_2 fraction, and consequently, a standard of 30% H_2 was chosen for wafer fabrication in order to provide reasonable process latitude.

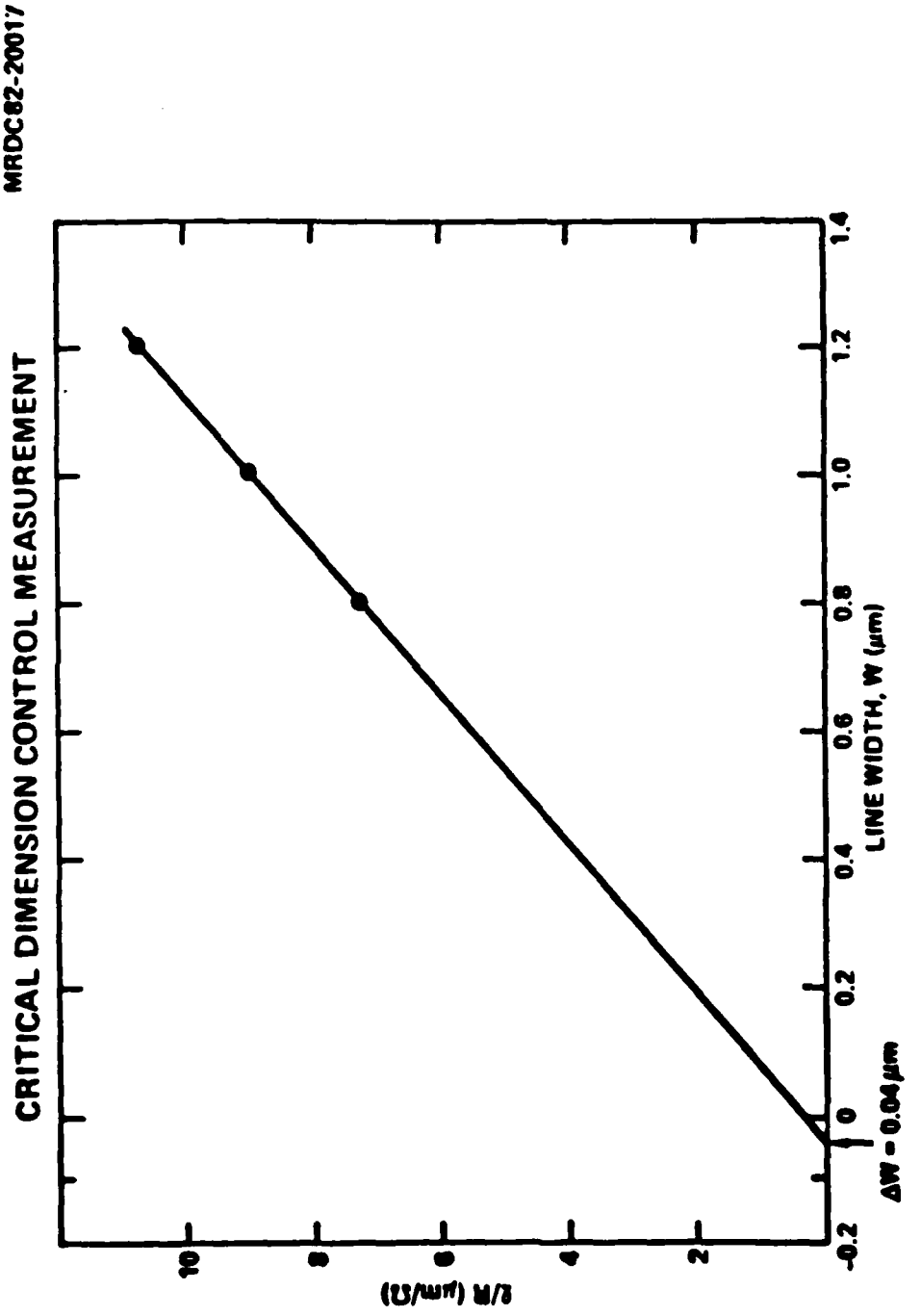

Fig. 4.6-4 Results of width measurement on metal lines fabricated by a plasma etched lift-off process.

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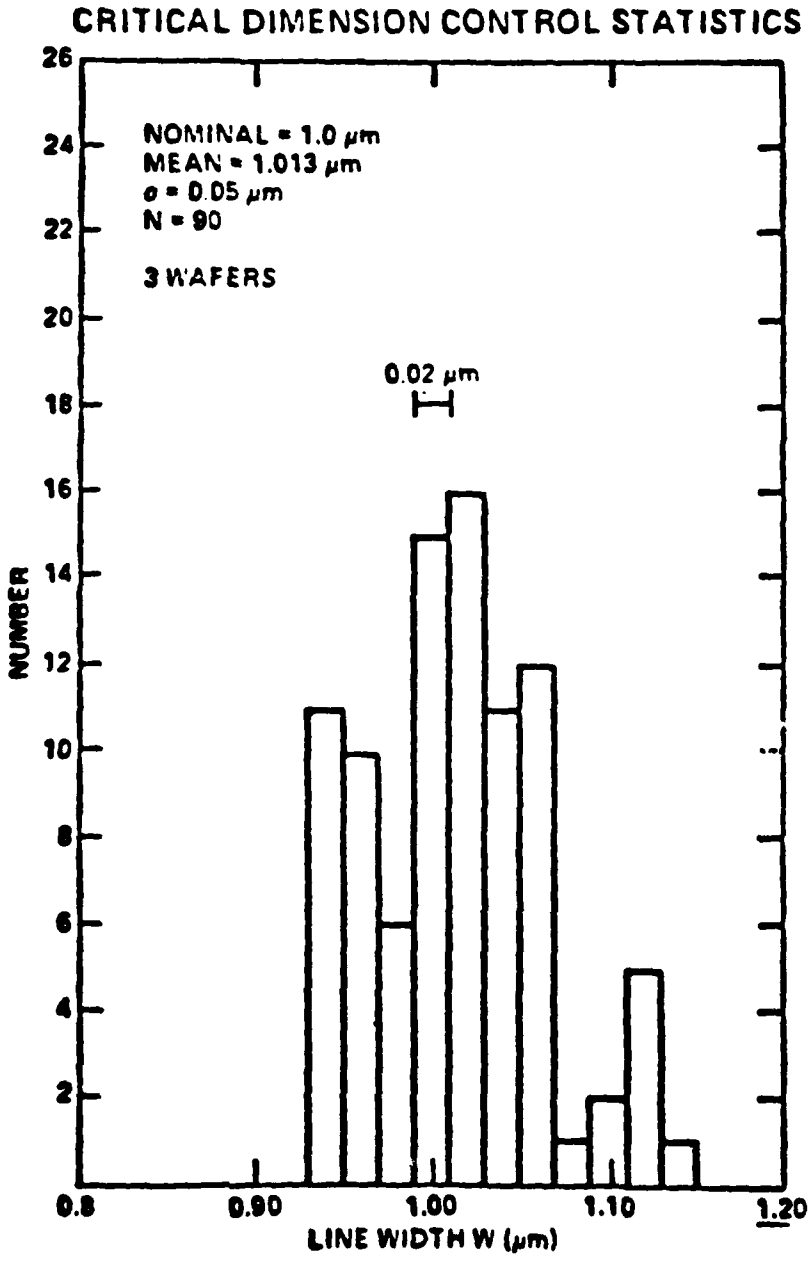

Fig. 4.6-5 Histogram of linewidth for metal lines of 1 μm nominal width.

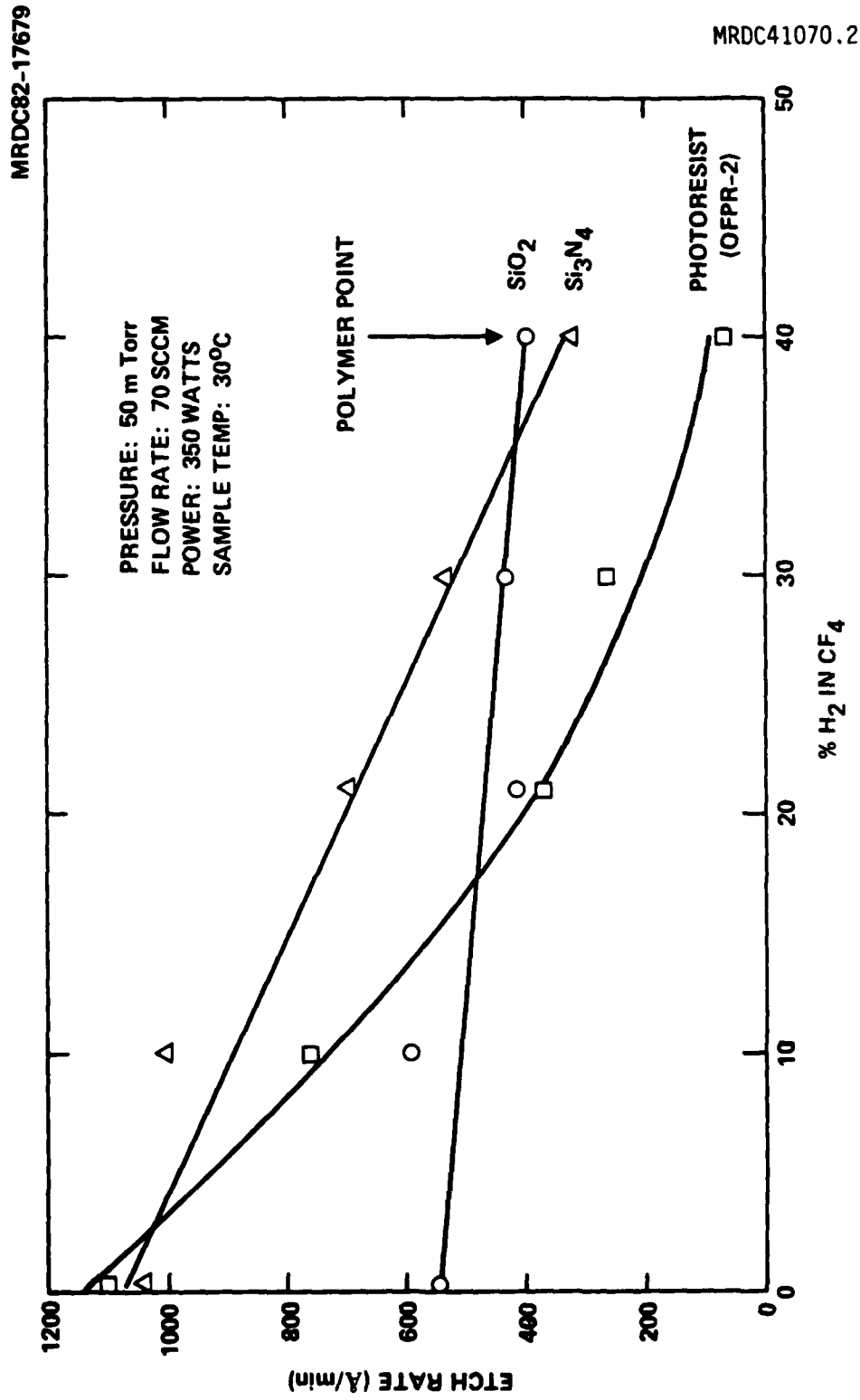

Fig. 4.6-6 Etch rates of SiO_2, Si, H_2 and photoresist as a function of H_2 fraction.

In addition to the etch rate studies, etch uniformity was also investigated using both the standard LPCVD SiO_2 layer as well as a phosphorus doped glass (PDG) layer. The results of the measurements are shown in Fig. 4.6-7. The uniformity of the etch across a 3-in. wafer is very good with both materials. PSG offers the advantage that its higher etch rate will allow an even greater selectivity with respect to photoresist loss. Therefore, PSG is a possible candidate to substitute the LPCVD SiO_2. However, it has not been incorporated into the mainline process.

In preparation for the launch of the 3 inch wafer process, the uniformity of SiO_2 depositions both by sputtering and by low-pressure CVD were verified, and so was the uniformity of metal depositions both by magnetron sputtering and e-beam evaporation. As shown by the data in Figs. 4.6-8 and 4.6-9, the uniformity obtained across the diameter of 3 inch wafers is good.

4.7 Fabrication of 3-inch GaAs Wafers

The implementation of the processing of 3 inch wafers was very successful. The vehicle chosen was mask set RM3 containing 256 bit GaAs static RAMs and designed under another DARPA sponsored program.[16] The fabrication process for 3 inch wafers is identical to the process used for 1 inch square wafers.[1] Differences can be found only in the equipment used. The 3 inch wafer process required a significant amount of equipment upgrading and replacement, the most important item being the photolithography equipment discussed in Section 4.6.

At the end of this program, 6 lots of 4 wafers each had been fabricated. Breakage was at this stage a rather serious yield limiting factor causing the loss of 31% of the wafers. However, breakage occurred only at a few specific process steps, and it was quite clear that significant breakage reduction was possible by simple improvements in wafer holding fixtures within some of the equipment. A reduction of breakage to a still high but acceptable 10% is forecasted. Other causes of catastrophic failures were traced to dielectric adherence which caused a loss of 6% of the wafers. The yield of good dies on the wafers was not 100% due to gross misalignment of some dies.

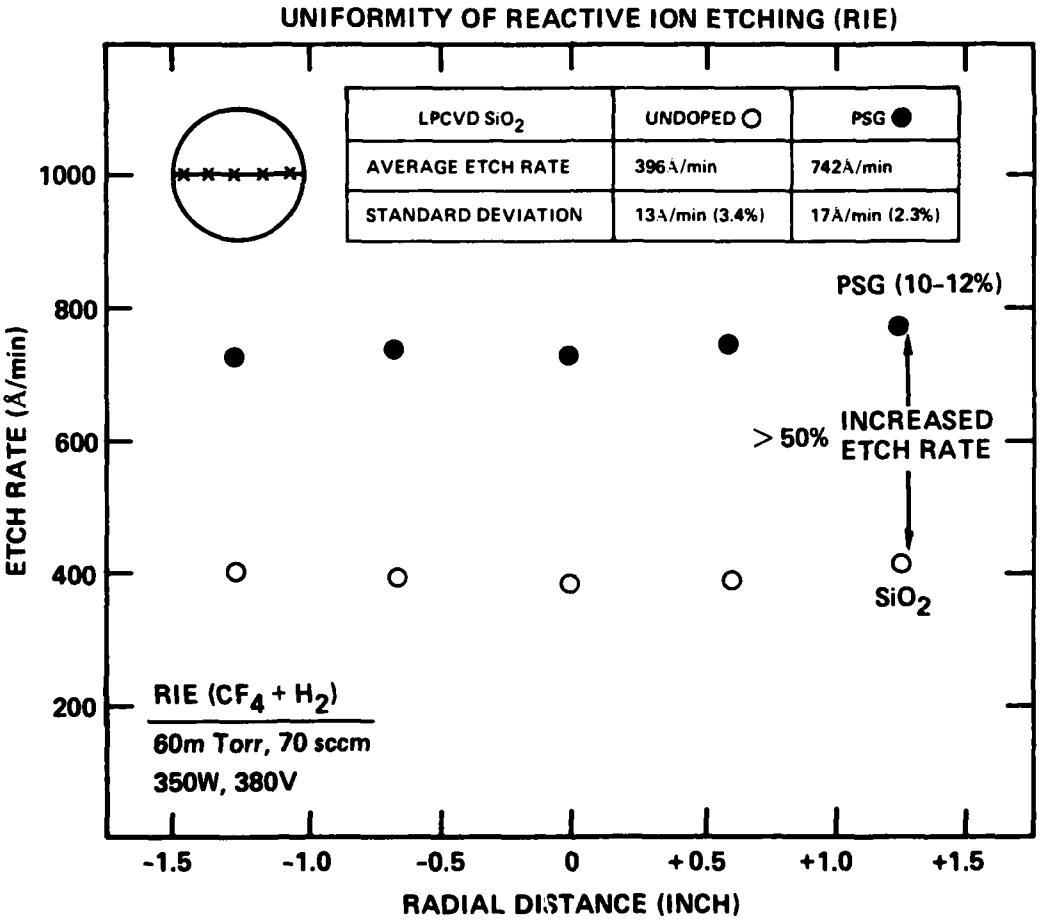

Fig. 4.6-7 Uniformity of reactive ion etching (RIE).

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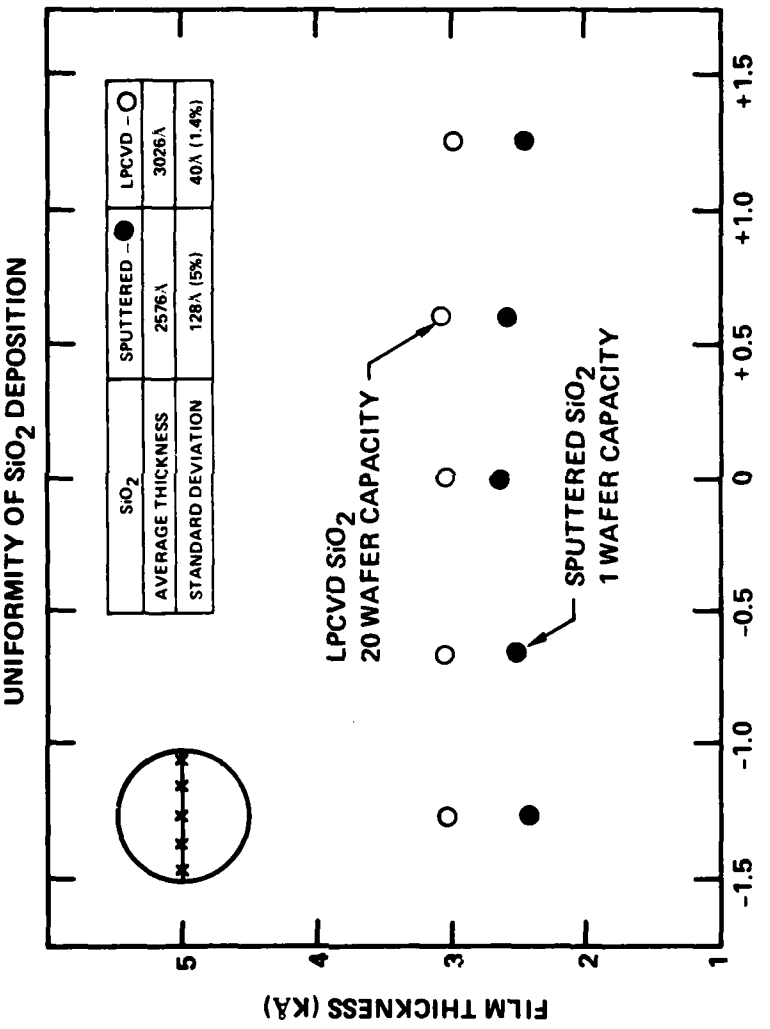

Fig. 4.6-8 Uniformity of sputtered and chemical vapor deposited SiO_2 across the diameter of a 3 inch wafer.

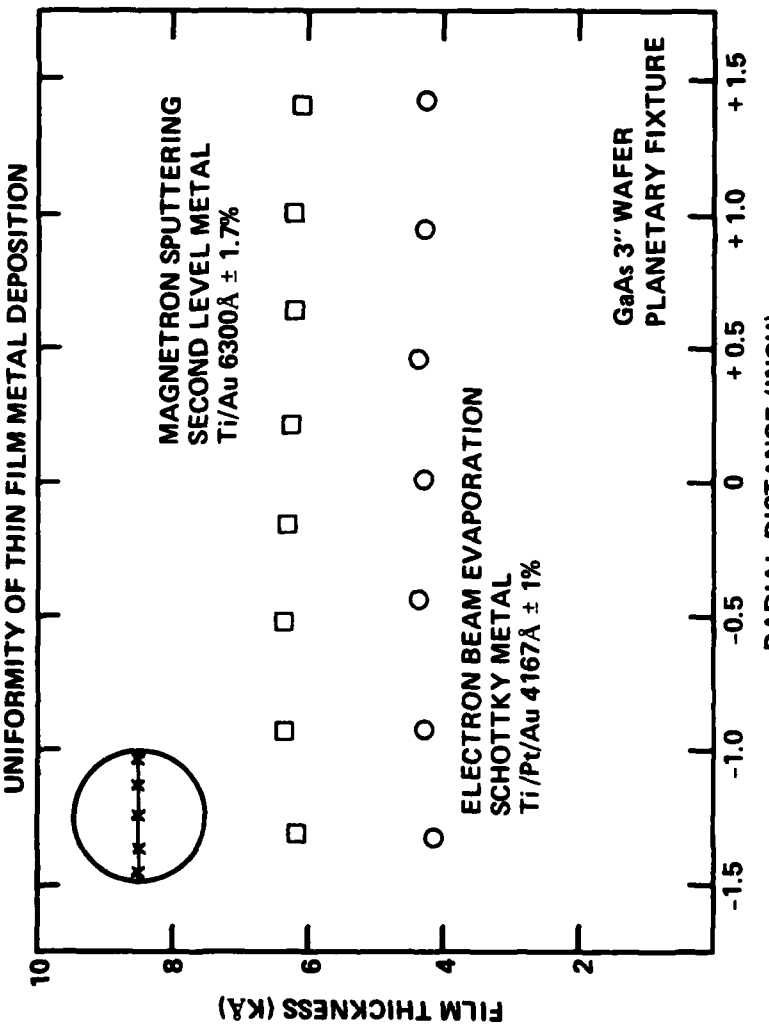

Fig. 4.6-9 Uniformity of magnetron sputtered and E-beam evaporated metal layers across the diameter of a 3 inch wafer.

However, it was obvious that simple improvements in the design of alignment marks could easily eliminate this deficiency.

While the successful results obtained from testing the 256 bit RAMs are discussed elsewhere,[16] data from parametric testing contribute some direct information on the status of the fabrication process. Ohmic contact uniformity was found to be excellent. Figure 4.7-1 displays a histogram from ohmic contact test structures across a 3 inch wafer showing a standard deviation of contact resistance of only 14% of the average, which corresponds to a specific resistance of 1.3×10^{-6} Ωcm^2.

Depletion voltage measured by C-V profiling show excellent uniformity of the implants, with a 69 mV standard deviation of the depletion voltage (Fig. 4.7-2). Wafer maps of FET threshold voltage (Fig. 4.7-3) and saturation current (Fig. 4.7-4) also show good uniformity. The threshold voltage of approximately -1V, shows a standard deviation of 130 mV (13.2% of the mean) while the corresponding standard deviation of I_{dss} is equal to 11.4% of the mean. Equally good results were obtained from test diodes, ohmic contact structures, etc.

In general, FET threshold voltages and saturation currents tend to show systematic radial trends (Figs. 4.7-3 and 4.7-4). This systematic behavior will require further investigation. Corrections of these trends could lead to significant improvements in device uniformity.

The mean FET threshold voltage is displayed in Fig. 4.7-5 as a function of the test date, which is close to the fabrication date. The first two lots of wafers were deliberately processed for approximately -1 V threshold, while the following wafers were targeted for the -0.5 to -0.7 V range required for the low-power RAMs.[16] In Fig. 4.7-6, mean saturation currents are plotted against mean threshold voltages. The near quadratic relationship between these parameters which has been traditionally observed between I_{dss} and V_p is also observed here. If plotted together with previous similar data from 1-in. square wafers they would be on the same curve. This is an indication that the device characteristics have not changed, as it was expected.

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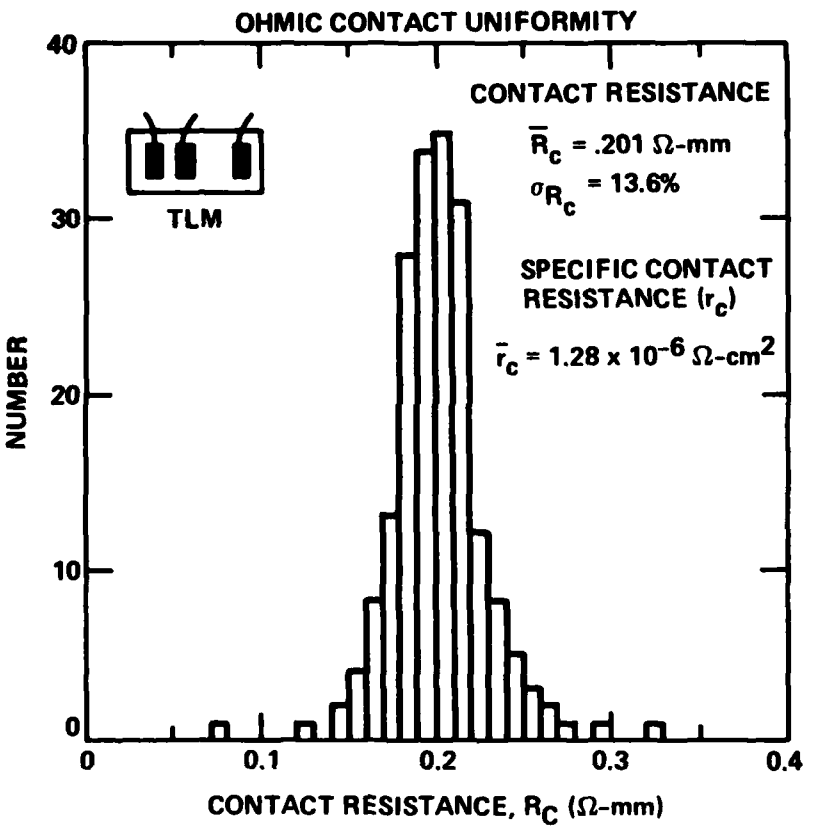


Fig. 4.7-1 Histogram of ohmic contact resistance across a 3 inch GaAs wafer.

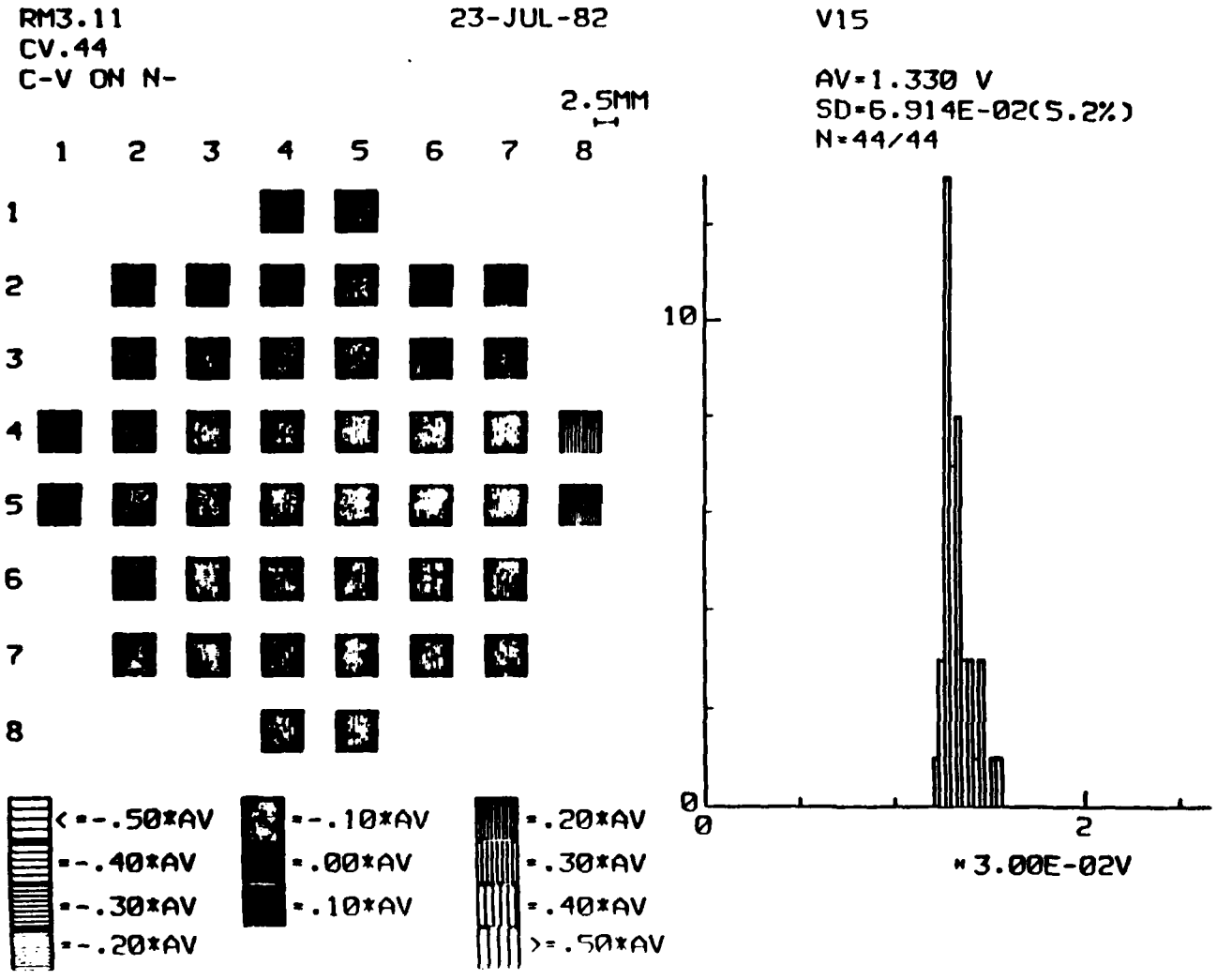


Fig. 4.7-2 Wafer map and histogram of depletion voltages across a 3 inch GaAs wafer. The depletion voltage is obtained by C-V profiling, and it is defined as the voltage corresponding to a 10^{15} cm^{-3} carrier concentration.

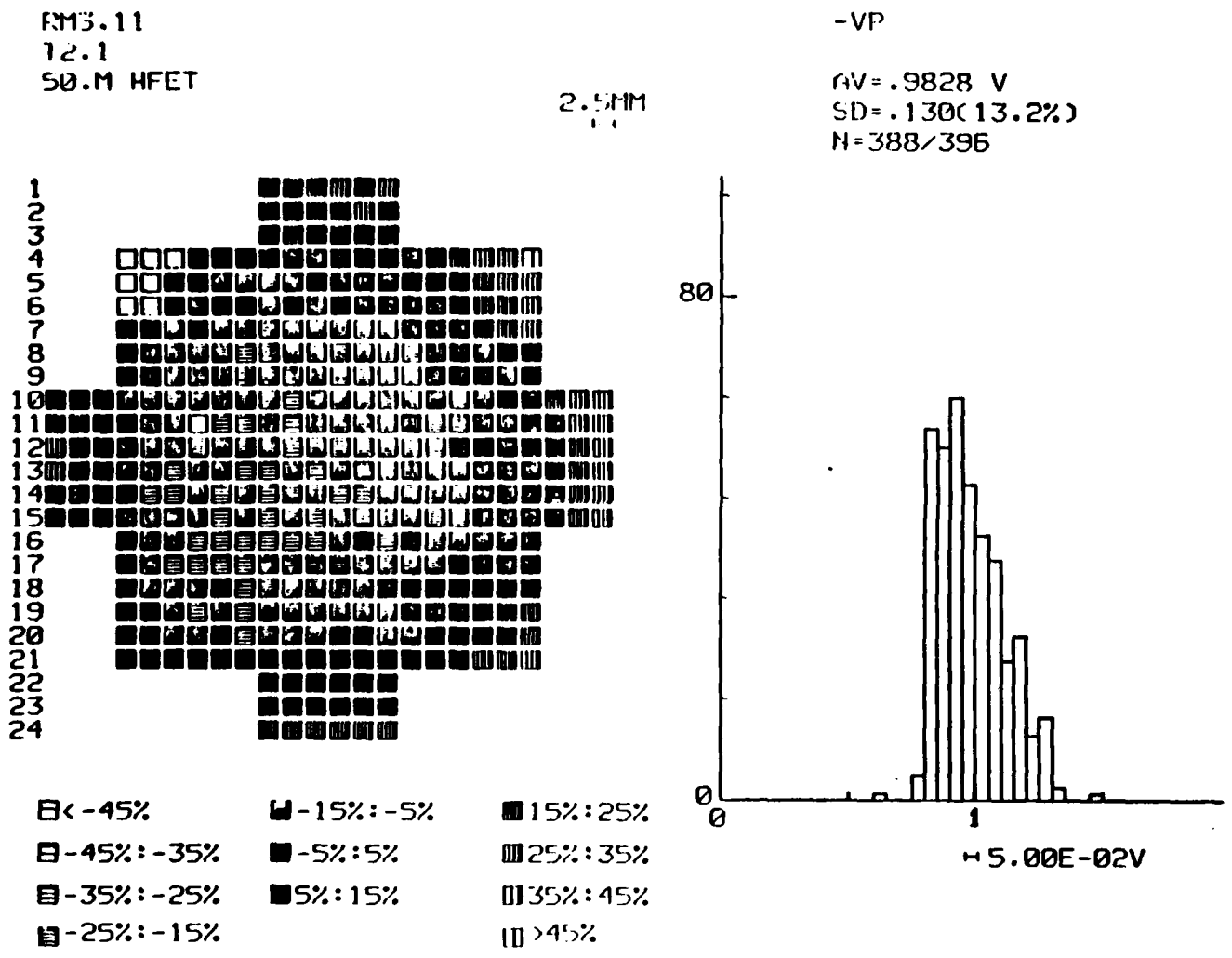


Fig. 4.7-3 Wafer map and histogram of FET threshold voltages for a 3 inch diameter GaAs wafer.

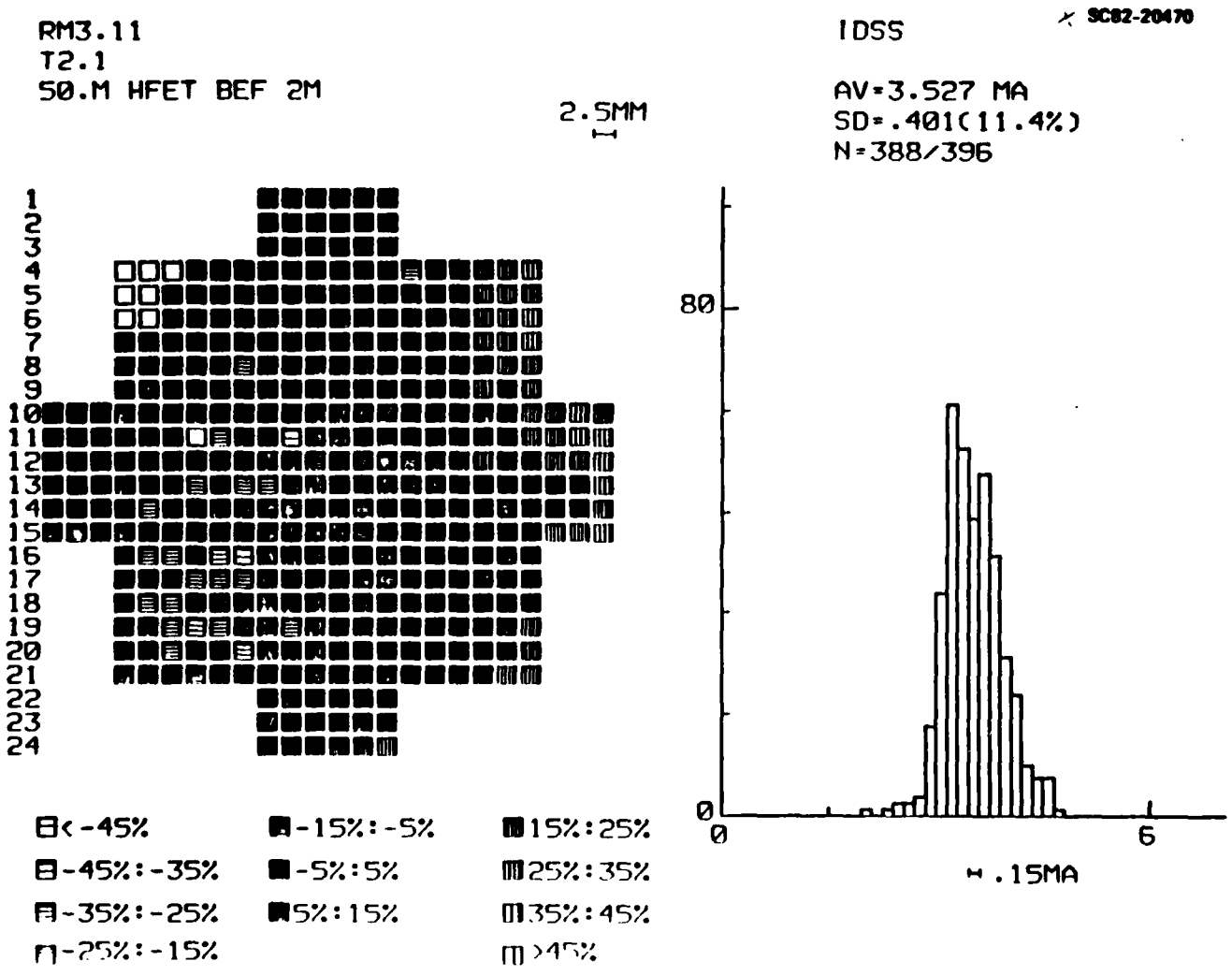


Fig. 4.7-4 Wafer map and histogram of FET saturation currents for a 3 inch diameter GaAs wafer.

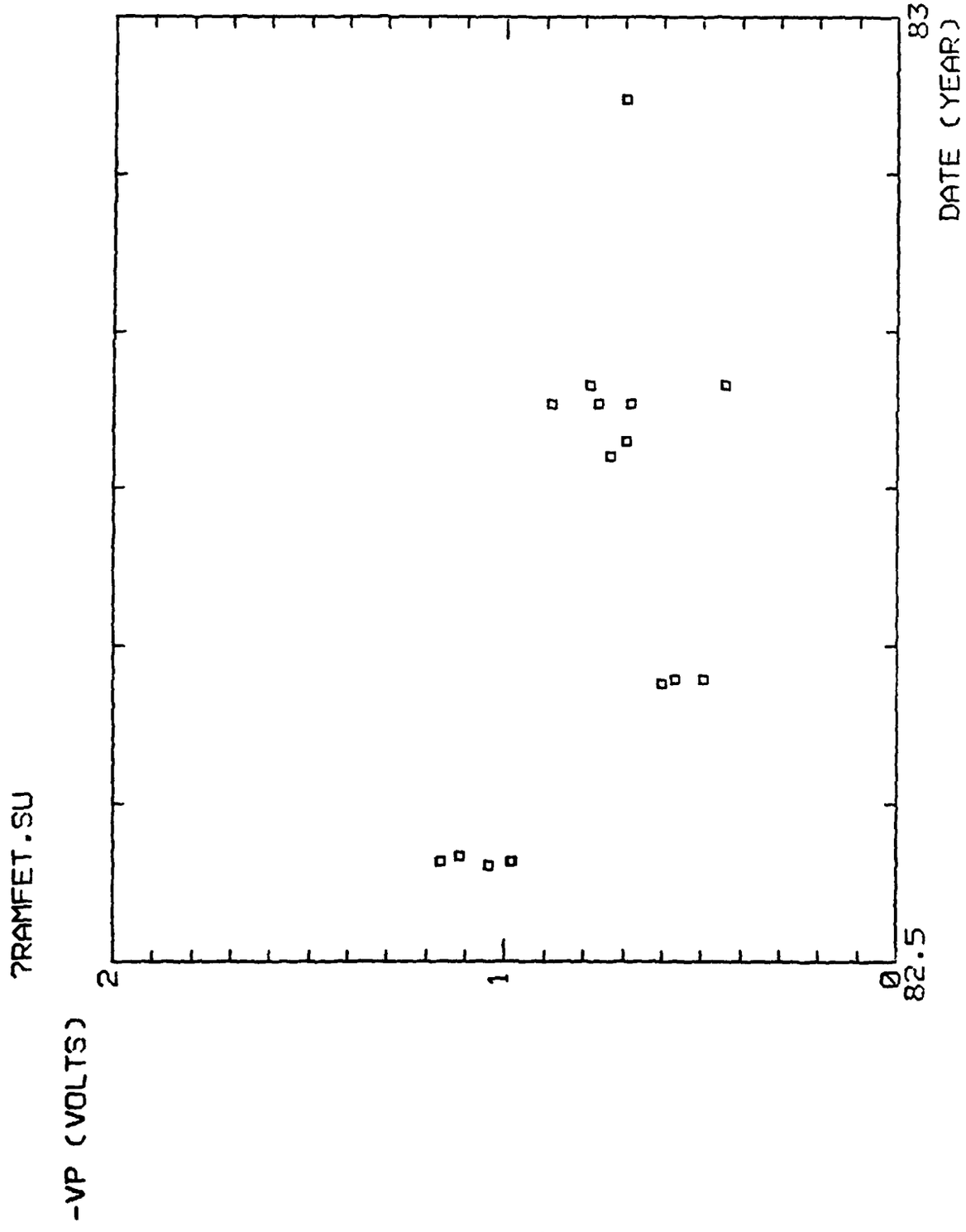


Fig. 4.7-5 History of mean threshold voltages of GaAs 3 inch wafers.

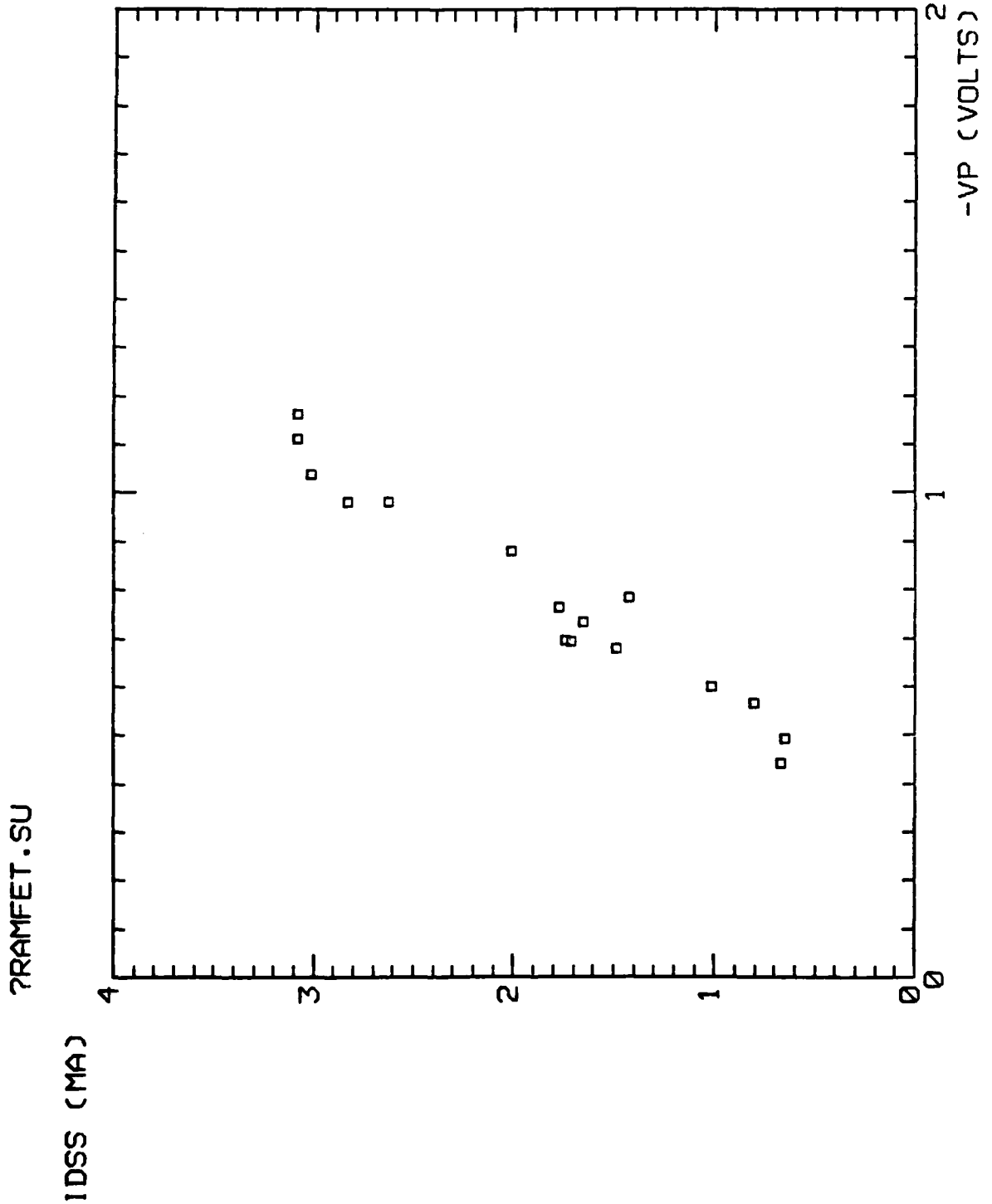


Fig. 4.7-6 Mean saturation current vs mean threshold voltage for 50 μm wide test FETs on 3 inch GaAs wafers.

In conclusion, the launch of the 3 inch wafer process was very successful. A number of second order problems such as breakage, alignments, etc. have been identified, and ideas on how to address them have been generated and proposed for a new phase of this program.

5.0 CIRCUIT DESIGN AND TEST

Although the main emphasis of this program was on process development, design and testing of GaAs integrated circuits was also an important task. All the work reported here was carried out using normally-on MESFET devices using Schottky Diode FET Logic (SDFL) gates as circuit building blocks. In the early part of the program, the evaluation of 8 × 8 bit parallel multipliers (1000 gate circuits) developed and fabricated under a previous program was completed. The circuit was found completely functional, and a best multiply time of 5.2 ns was determined. Since these results were discussed in the previous final report,[1] they are not repeated here. A new logic family called Schottky Diode Diode FET Logic (SD^2FL) which represents an expansion of SDFL was developed and evaluated. This work, discussed in Section 5.1, indicated that this new family can be very useful, but only for limited applications. Sequential circuits of the programmable pattern generator type were designed and tested (Section 5.2). Finally, the design of a family of mask programmable logic array meeting ERADCOM requirements was started. This activity, discussed briefly in Section 5.3, and more extensively in Appendix A, is expected to lead to the development of components for a frequncy synthesizer.

5.1 Schottky Diode-Diode FET Logic (SD^2FL)

A logic gate circuit design must be capable of extension to two or more levels of logic per gate delay in order to realize the highest speed, and to minimize chip area and power dissipation for a given IC logic technology (a logic level consists of one (N)AND or (N)OR operation of arbitrary width). Multilevel gate implementations allow complex logic operations to be achieved in slightly over one basic logic gate propagation delay (τ_d) rather than two or three delays as would be the case for single level NOR or NAND implementations. They also dissipate less power and require less wafer area than single level circuit implementations.

The use of combinations of series (NAND) or parallel (NOR) FET configurations to achieve two-level logic functions is common. VanTuyl, et al.[17] demonstrated depletion-mode GaAs MESFET buffered-FET logic (BFL) NAND/NOR (or

NAND/WIRED-AND) gates, with up to two NAND input terms (series or dual-gate FETs) and up to two of these NAND functions "drain dotted" together, having propagation delays as low as τ_d = 110 ps. Multi-level logic gate configurations may also be realized in SDFL with up to 3-level gates.[18] In the previously-published SDFL work,[18] the FET logic function utilized was principally the inverter, so that, with the diode-OR, a NOR gate function was realized (Fig. 5.1-1a). On the other hand, by using such diode-OR clusters on each gate of a dual gate FET (or series-FET connection), an OR/NAND 2-level gate is achieved (Fig. 5.1-1b), This gate is the complement of the 2-level NAND/NOR gate realized in BFL, except that the number of first level terms in the SDFL version is no longer restricted to two. The resulting OR/NAND function $F = \overline{(A+B+C)(D+E+G)}$ can be used to reduce considerably the propagation delay per equivalent gate by performing a two-level operation in approximately one NOR gate delay. Power dissipation is only slightly above that of a NOR delay gate (one added pull-down) and the area is also only slightly greater.

A three-level (OR/NAND/WIRED-AND) gate can also be constructed by the use of "drain-dotting" or sharing of a common pull-up by two OR/NAND gates. An example of this gate is shown in Fig. 5.1-1c. Again, the number of OR inputs is arbitrary. Here, the three-level logic function $F = \overline{[(A+B+C)\ \ (D+E+G)]} + \overline{[(H+I+J)\ \ (K+L+M)]}$ is performed by this gate in substantially the same propagation delay time required by a single NOR gate. Proper dissipation is again only slightly above that of a single level (NOR) gate, and the area would be about twice that of a NOR gate.

The multi-level logic gate approach described above allows major saving of chip area and power dissipation, and also increased circuit speed (fewer gate delays). In general, however, the numbers of terms which can be practically "NAND'ed" with series FETs without substantial performance degradation is limited to two due to parasitic gate capacitances and FET "ON" resistances. Similar restrictions apply to the "drain dot" -wired AND of the three level OR/NAND/WIRED-AND gate. To avoid this fanin restriction of multi-level logic gates, the extra fast logic element available in the GaAs Schottky diode can be utilized to perform two levels of logic operations rather than just one level. Figure 5.1-2 illustrates the use of 2 levels of diode logic

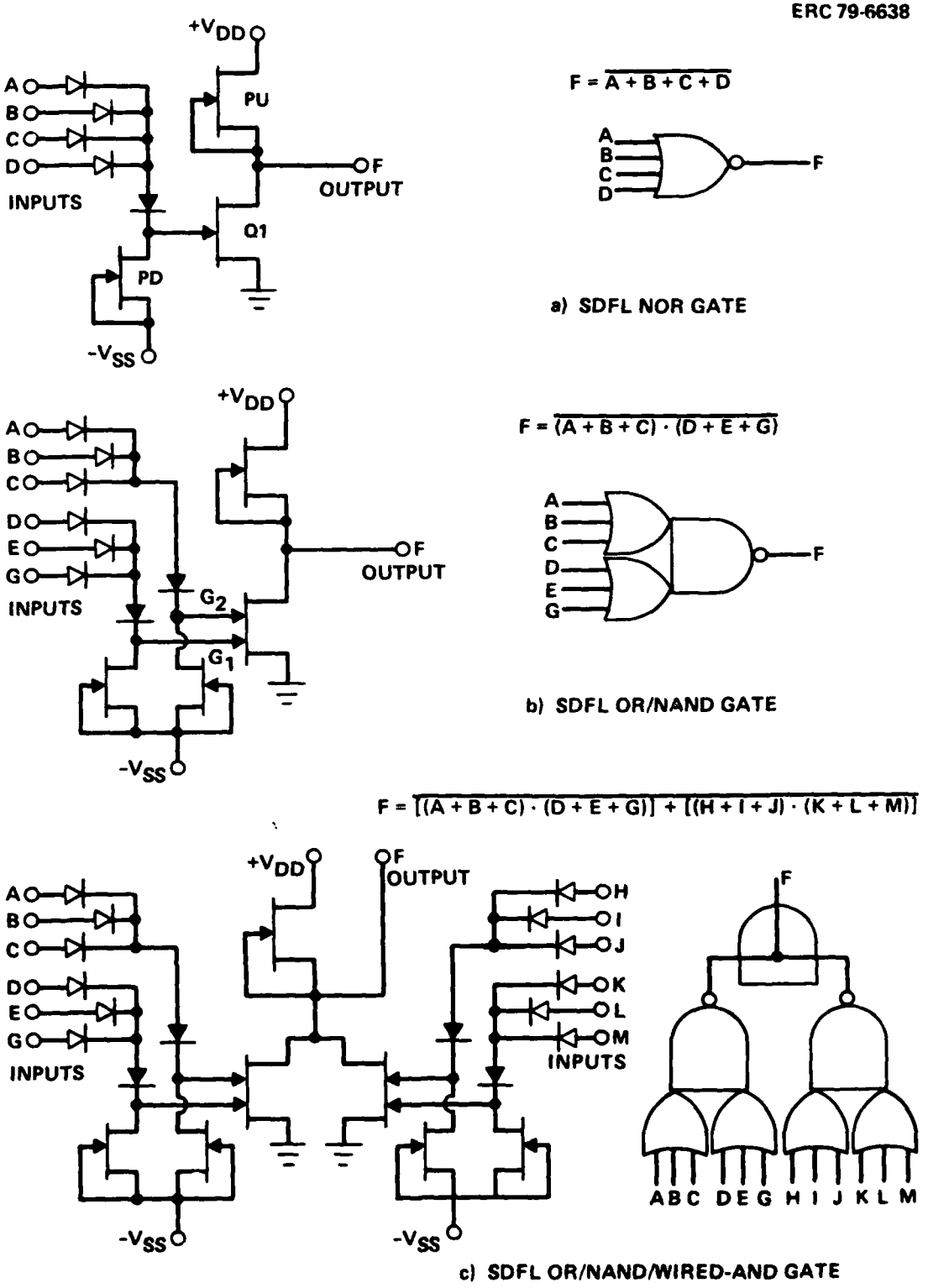


Fig. 5.1-1 Comparison of 1, 2 and 3 level SDFL gate configurations.

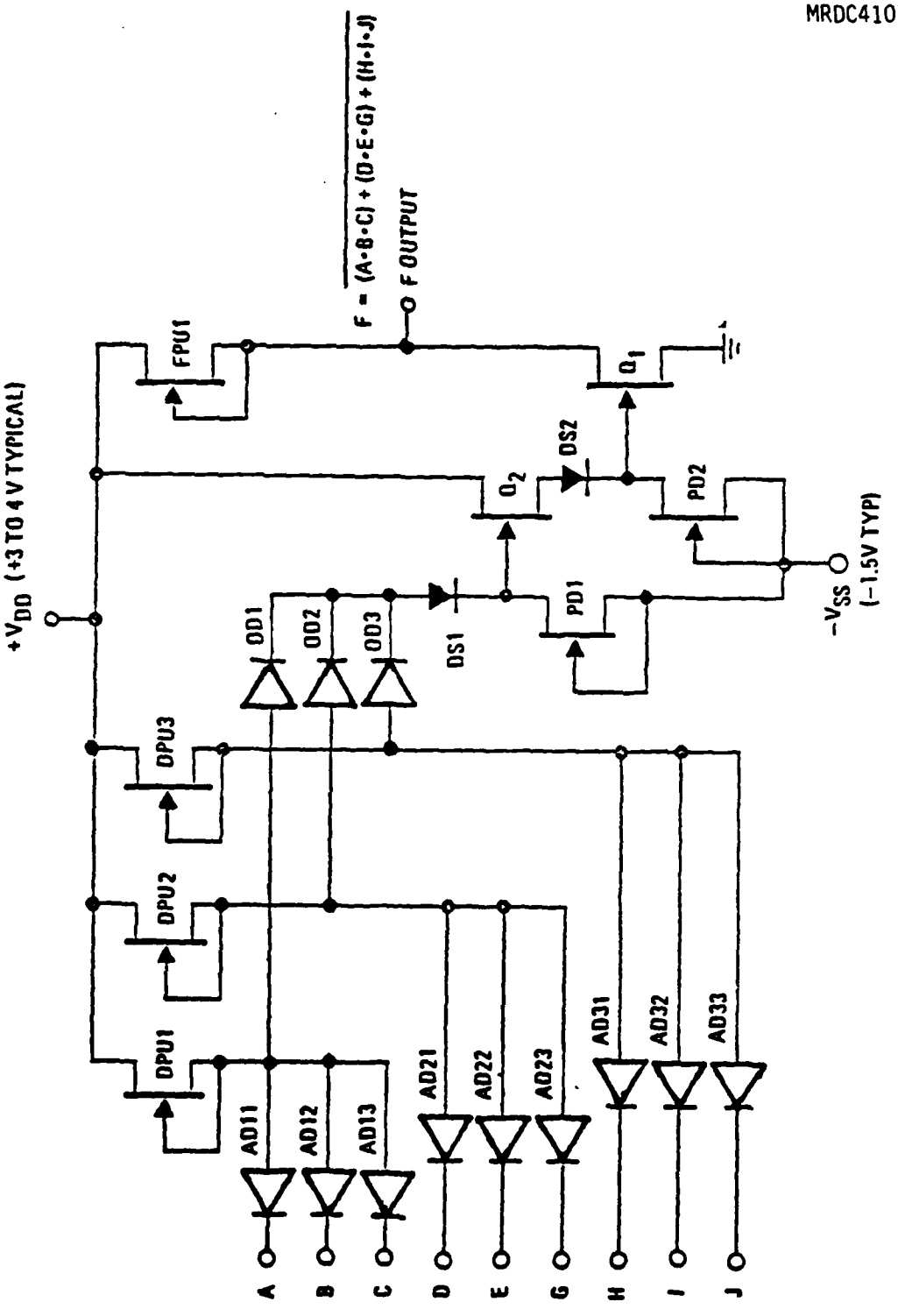
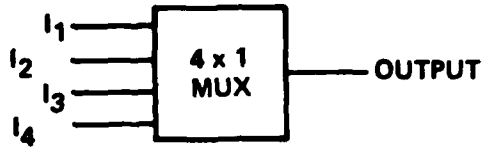


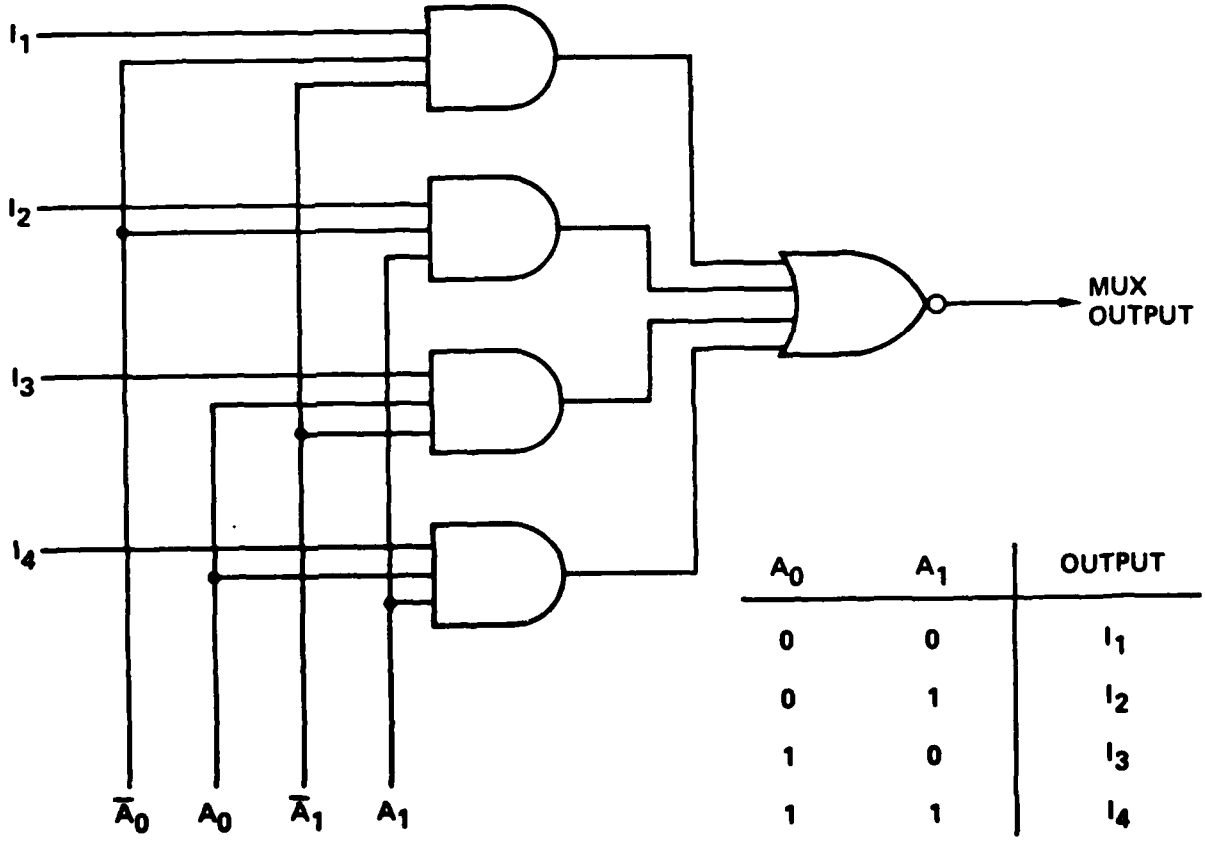
Fig. 5.1-2 Circuit diagram of simple Sn^2FL logic gate.

with the basic SDFL gate structure. Clusters of diodes (AD_{xx}) with their cathodes connected to inputs and their anodes connected in common to a pull up (DPU_x) form the first level of positive - AND function (i.e., if any input is "low" the common anode must be low). The anode output of these AND clusters are combined to form an "OR" diode cluster (OD_x) and the common cathodes of this diode cluster are connected to the FET (Q_1) gate and its pull down current source, PD1, through two voltage level shift diodes (SD1, SD2) such as would be needed in a regular SDFL gate.

Figure 5.1-3 illustrates how this type of simple 2-level diode logic (SD^2FL) gate can be utilized in a typical application. With two levels of logic (AND-OR) and unlimited width (as compared to the FET NAND or "drain dot" which is typically limited to 2 or 3 terms), most desired logic functions can be directly obtained from their full min-term expansion in only one gate delay. In the 4 to 1 multiplexer example of Fig. 5.1-3, it only takes one SD^2FL logic gate and one gate delay to generate this function which would require five SDFL NOR gates and two NOR gate delays to realize in single level logic. The SD^2FL gate in this example, therefore, has an equivalent gate count of 5.

Unfortunately, in the simple SD^2FL version of Fig. 5.1-2, the speed advantage will be lost because of the unfavorable ratio between the pull down size (W_{PD}) and the width of FET (W_Q) which must handle all of the diode pull up currents. With a fan out of 6, a ratio of $W_Q/W_{PD} = 20$ is required. This 20 to 1 ratio would lead to gate delays up to 4 times worse than an SDFL NOR gate in which the W_Q/W_{PD} ratio is usually kept at 5:1. Figure 5.1-4 shows an improved version of the 2 level diode logic gate which would allow an implementation of complex circuits without gross speed loss due to fan out drive problems. The key to this improved SD^2FL circuit speed is the inclusion of the source follower driver stage (Q_2-PD_2) to provide current gain from the small logic diode current levels up to the substantial gate drive currents required for the high speed switching of Q_1. With the sacrifice of slightly increasing the power dissipation and complexity (due to the addition of the source follower driver), the gate delay time of the modified SD^2FL gate should be nearly as fast as the SDFL NOR gate.





A_0	A_1	OUTPUT
0	0	I_1
0	1	I_2
1	0	I_3
1	1	I_4

Fig. 5.1-3 Logic diagram of 4 to 1 multiplexer realized with a single SD^2FL.

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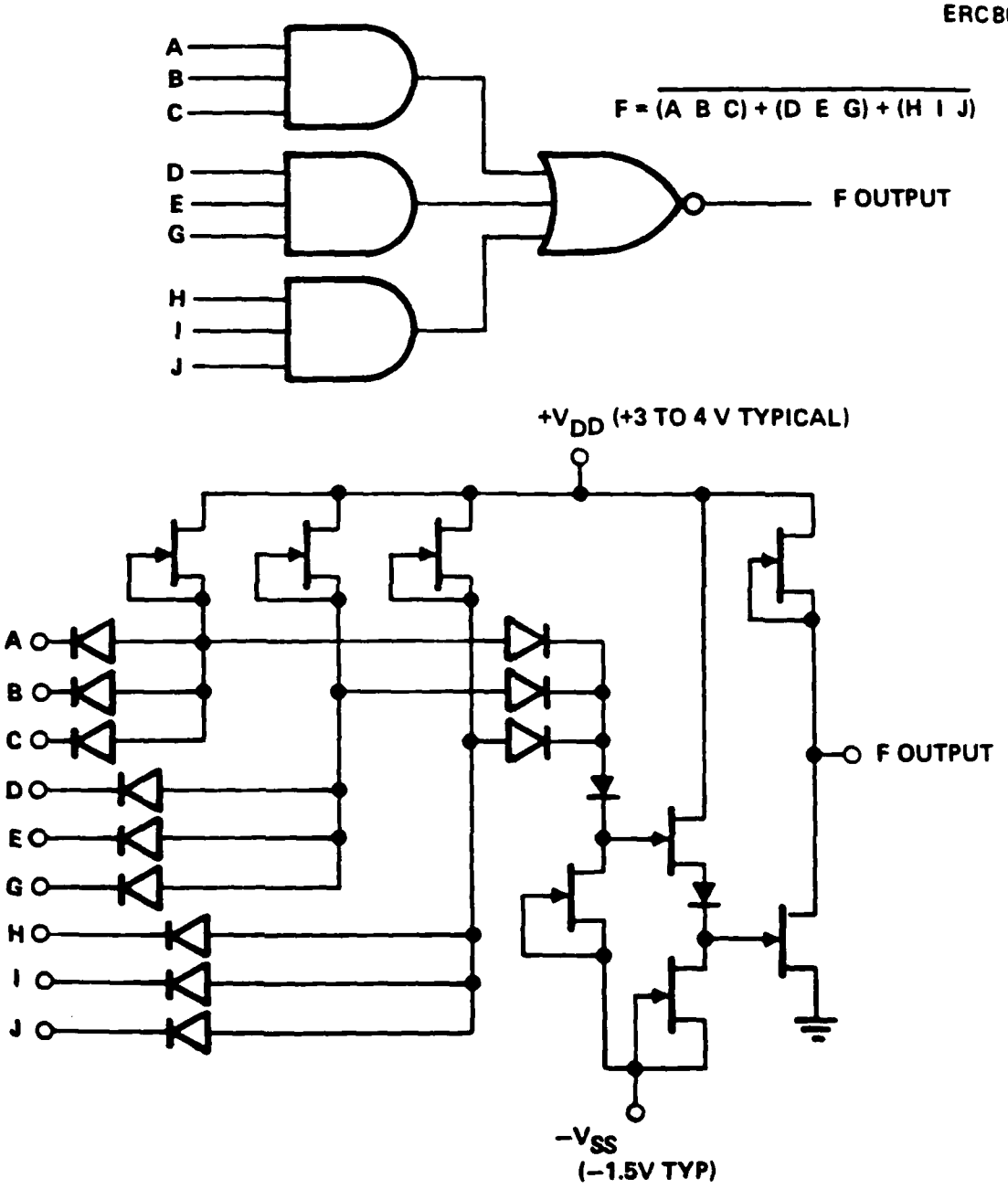

Fig. 5.1-4 Schematic of an improved version of the Schottky diode-diode FET logic (SD^2FL) gate.

The extension of this SD^{2}FL approach to an even higher level of logic function can be easily achieved. Note that if Q_1 is a dual gate FET and if the input and same source follower structure is used for each gate, a 3 level gate AND/OR/NAND gate will be obtained. Similarly, if another such 3 level gate were connected with their outputs sharing a common pull up, a 4 level AND/OR/NAND/ WIRED-AND would be obtained.

An 8 × 8 bit parallel multiplier was chosen as a vehicle to test SD^{2}FL. The architecture is the same simple ripple type previously used with SDFL: so that conclusions could be drawn about the efficiency of the SD^{2}FL approach compared to the SDFL approach. The 8 × 8 multiplier was designed using two-level, Schottky Diode-Diode FET Logic (SD^{2}FL) gates to implement the adders in the multiplier array. The compelling feature of these gates is that a full adder cell implemented with four of them provides both sum and carry outputs with a propagation delay equal to only one gate delay (τ_d), rather than the average 2.5 τ_d of a SDFL full adder. The circuit structure of the SD^{2}FL gate is slightly more complex than that of a SDFL gate, resulting in a τ_d for a SD^{2}FL gate that is approximately 1.5 times that of a SDFL gate. This is a result of the increased capacitance due to more diodes at the logic summing mode, and the delay of the additional source follower stage used to discharge the gate of the switching FET. Therefore, the speed advantage of the SD^{2}FL adder, compared to an (average) SDFL adder, is on the order of 1.7 times.

Preliminary estimates were previously made of the packing density and power dissipation of a SD^{2}FL multiplier that would achieve this increase in speed. These preliminary estimates indicated that along with the increase in speed, there would result a decrease in layout area, as well as a decrease in power dissipation. However, the detailed circuit design and layout performed for the multiplier established that the reduction in area for the 1 τ_d adder is not as much as estimated earlier, and that the power dissipation is substantially greater when appropriate transistor sizes are selected for the increased speed (compared to the NOR gate SDFL implementation). With the design

essentially complete, size and power estimates resulted as follows: 1) the size of a SD^2FL full adder is approximately 90% of that of a SDFL adder; 2) its power dissipation, which, unlike that of the NOR adder, is constant,* will exceed the average power of a NOR adder by 92% (or 1.92 times), and will exceed the maximum power of a NOR adder by 35%; 3) additionally, relative to size, the increased power dissipation necessitates an increase in power bus line areas that nearly cancels the 10% area saving when equal current densities are maintained. These figures apply while realizing the estimated 70% increase in speed. A one-line summary is that the SD^2FL multiplier realizes a 1.7 times increase in speed, less than 10% saving in chip area, with nearly twice the power dissipation of a NOR implementation.

At this point, it is worth considering the discrepancy between expectation and realization of area and power. When the completed design is examined, it becomes clear that an array multiplier circuit benefits less than almost any other logic circuit from a SD^2FL implementation, compared to a straight NOR (SDFL) one. The predominant reason is that both true and complement values of the sum and carry outputs of each adder must be both generated and routed as interconnections in implementing full adders. Thus, the gate count is increased, as well as the routing area. SD^2FL gates are larger than SDFL gates, in order to drive the greater capacitance of the greater number of input diodes; also, to assure switching under worst case conditions, it is necessary to increase the sizes of the input diodes, further increasing input capacitance and, hence, gate size.

Of the four gates that generate the sum and carry and their complements, clearly two must always be "on." The power dissipation is not only constant, but equal to that of the larger gates. The net result is the minimal benefit in area and penalty in power mentioned above.

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*The power is constant because for each of the sum and carry outputs, both true and complement are provided; thus one and only one gate of each pair is always on.

The conclusion is that the AND-NOR combination is not very efficient for arithmetic functions. The basis of arithmetic is the exclusive-OR function. Implementing an exclusive-OR with a minterm expansion in the SD^2FL gate involves the maximum number of combinations of true and complement variables; e.g., for three variables, the sum output is

$$S = A\overline{BC} + \overline{A}B\overline{C} + \overline{AB}C + ABC \qquad (2)$$

None of the reductions ordinarily encountered in the case of more general logic functions is possible. Thus, in terms of interconnections and numbers of inputs, the adder array used in the multiplier is one of the most complex circuits that could be selected for implementation with SD^2FL gates. By comparison, the SDFL NOR gate implementation is a fairly efficient one; only two (true) outputs are generated, minimizing interconnect area and the number of driver gates. The input fan-in is low, so that driver gates are small. Thus, the area and power of the AR5 SDFL multiplier have been minimized for an implementation that is efficient in terms of those (area and power) parameters. This efficient application of the NOR gates is being compared to a much less efficient implementation with SD^2FL gates. If a comparison were made with an SDFL version in which true and complement of sum and carry outputs were generated and routed (so that the comparison would be for functionally equivalent circuits), the area and power savings of SD^2FL would be obtained. The area and power savings should also apply when implementing logic functions other than arithmetic.

As an example of a circuit that is efficiently realized with SD^2FL gates, consider the multiplexer circuit discussed earlier in this section and shown on Fig. 5.1-3. It can be implemented with one SD^2FL gate, or 5 SDFL NOR gates. Area and power savings for this example are dramatic. The area of a SD^2FL gate is approximately 4500 μm^2, or 46% of the 9600 μm^2 occupied by a 5 gate equivalent. The power dissipation of the one SD^2FL gate in only 40% of the power in a 5 gated equivalent, when equal loading is considered.

The 8 × 8 multiplier was digitized with the same peripheral latch circuits that were used on the previous SDFL multiplier. A photograph of the chip is shown on Fig. 5.1-5.

The full 8 × 8 multiplier was a very complex and large chip, which has the following impact on testing. First, the bias sensitivities of the two types of gates (SD^2FL and SDFL) were expected to be slightly different. Secondly, the yield on such large chips was anticipated to be low enough that a considerable number of chips would need to be tested to find fully functional ones. This testing would be made more difficult by the uncertainty of proper bias voltage conditions.

To overcome these potential testing limitations, the multiplier was designed with an alternate second metal mask that eliminated the latches, and subdivided the array into four smaller arrays (two 4 × 4 and two 3 × 4 arrays). This alternate connection layer would be used on the first lots of wafers to facilitate testing on the smaller SD^2FL arrays, which should have higher yield of working arrays, with outputs directly measurable so that bias voltage effects could be observed. Later lots would be processed with the fully connected mask layer.

Testing was started by checking a few circuits for functionality, using a ripple test, while adjusting voltages. From these, a number were identified that had no shorts, showed some degree of functionality, and exhibited output waveforms with well defined voltage levels. These were then tested in more detail, using the lower order bits in the upper right-hand corner. In Fig. 5.1-6 a functional diagram of the upper right corner, and the elements involved are shown. Specifically, the gate that combines a_0 and b_0 to form the LSB of the product, P_0 is a SDFL gate, so that SDFL performance can be evaluated. The gates and adders that form P_1 and P_2 are completely SD^2FL. The number of data paths is limited, so that correct operation can be verified; there are 32 unique combinations for this adder circuit. Unfortunately, under testing, it was found that lack of access to circuit nodes make it difficult to identify specific faults. For example, P_1 is the sum

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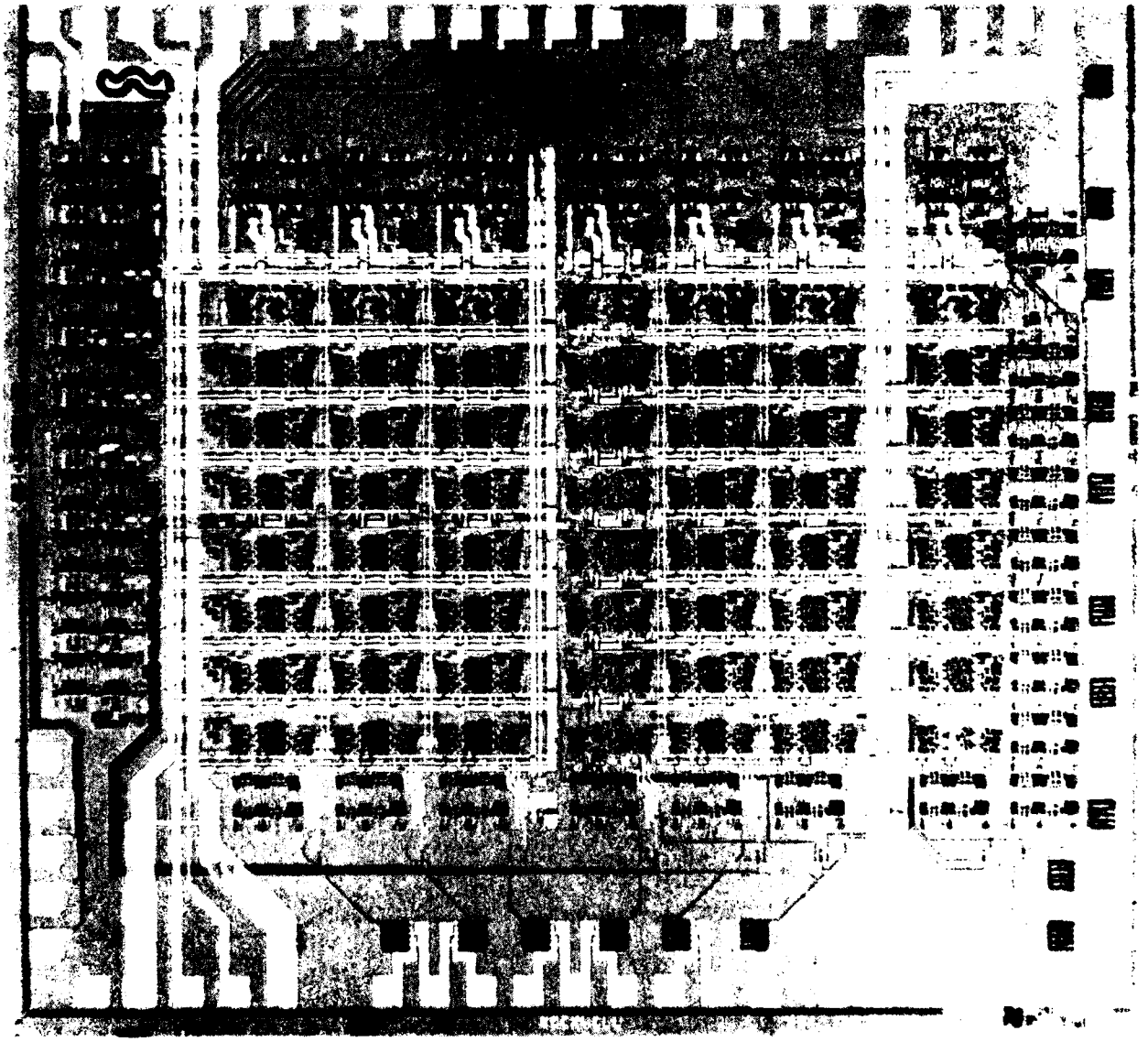

Fig. 5.1-5 Photograph of the 8 x 8 bit parallel multiplier chip.

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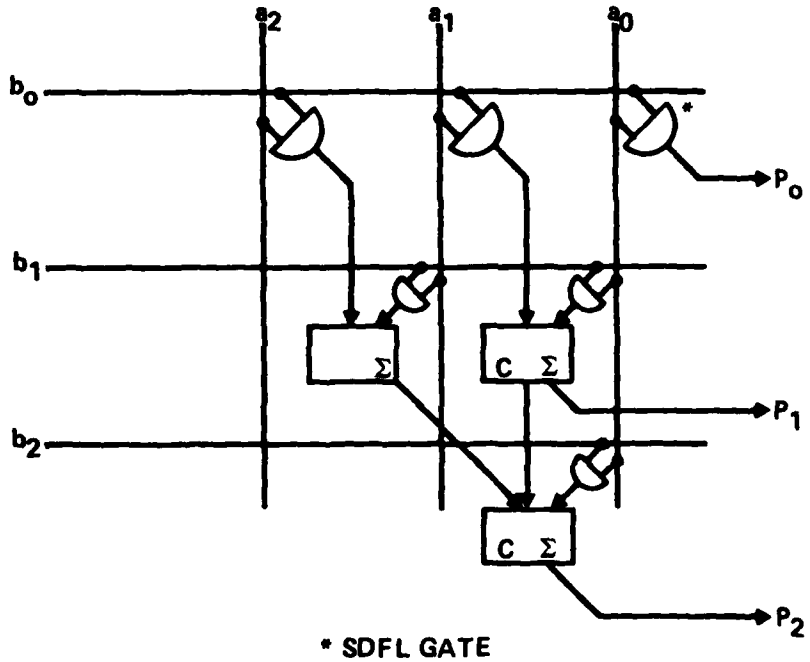


Fig. 5.1-6 Schematic of upper right corner (low order bits) of the SD^{2}FL multiplier.

output of a single field adder; its operation can be verified for the sum, but not for the carry. Similarly, the other adders are not fully accessible.

The adder corner combination was tested on several chips, for all input combinations, with varying bias conditions. The chips tested were selected for well defined output levels. None of the chips functioned completely. The failure were not consistent between input combinations; in some cases, for example, several combinations would produce an erroneous output only if a single gate had failed, but several other combinations would produce outputs that required that same gate to function. The testing was carried out to the point where it was suspected that voltage variations within the circuit during operation were affecting operation of some gates.

Testing of SD^2FL gates on previous mask sets has shown that the SD^2FL gate can operate as designed. The testing on AR6 has shown that an SD^2FL adder also operates. It is evident that cascading them results in interactions that have not been considered in the design. It is suspected that design and layout changes made with the intention to improve performance may be related to the failures.

Since the revised performance predictions discussed earlier did not indicate sufficient advantages for the SD^2FL design over a simple SDFL multiplier, efforts to further investigate the cause of the failure were not continued.

In conclusion, the SD^2FL gate can be implemented (despite the lack of success with the SD^2FL multiplier). However, it is advantageous only in certain specific cases where its large ANDing capability can be exploited. This is the case in the low-power GaAs static RAM, where SD^2FL gates were successfully used in the address decoder circuits.[19] However, a widespread use of SD^2FL circuits, as it was attempted on the 8 × 8 bit multiplier, is not advisable.

5.2 Sequential Circuits

A programmable linear feedback shift register (LFSR) was selected as a demonstration circuit because of important potential system applications. This circuit produces a binary sequence of length 2^m-1, where m is the number of stages. There are 2^m-1 possible initial loading conditions where each loading results in a distinct output sequence. Binary linear feedback shift registers can also be used to perform polynominal division, where all polynominals have coefficients that are either one or zero. When a linear feedback shift register (LFSR) is used for division, its feedback connection polynominal is defined as the divisor polynominal. To perform division, the registers in the LFSR should be cleared to zero. Then the polynominal to be divided is fed sequentially into the input of the LFSR with the most significant coefficient first. The quotient polynominal appears at the output of the LFSR as the input polynominal is being divided. After the input polynominal has been entered into the LFSR, the remainder polynominal or residue is left in the shift register stages.

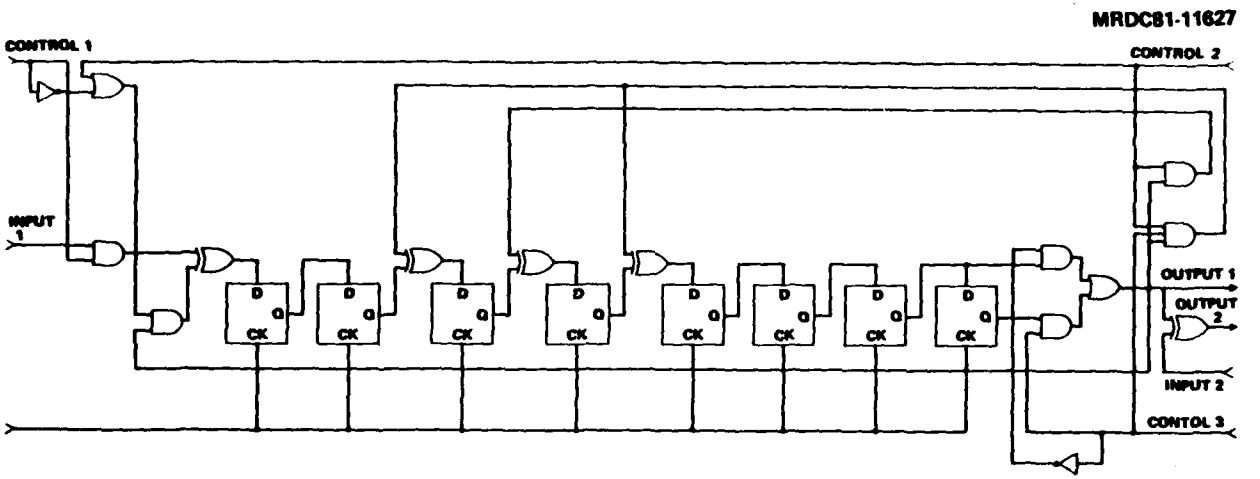
A programmable shift register/pattern generator was designed on the same mask set (AR6) used for the 8 × 8 bit SD^2FL multiplier (Section 5.1). The circuit generates an m-sequence (m = 7 or 8) P/N code or performs polynomial division. When used as a binary m-sequence code generator, the m stage shift register with feedback polynomial generates a distinct output sequence for each of the 2^m-1 possible initial conditions. The shift register is configurable in order to generate two distinct m-sequences. For m = 7, the seven stage shift register has a feedback polynomial of $x^7 = x^3 + 1$, and is capable of generating a binary P/N code of length $2^7 - 1 = 127$. For m = 8, the eight stage shift register has a feedback polynomial of $x^8 = x^4 + x^3 + x^2 + 1$, and is capable of generating a binary P/N code of length $2^8 - 1 = 255$. By using the two synchronized shift registers, whose lengths are relatively prime and whose feedback polynomials are different, a gold-code sequence with a period of $(2^7 - 1)(2^8 - 1)$ can be generated with the addition of an exclusive-OR output gate.

When used to perform polynomial division, the m stage shift register should be first cleared to zero. The polynomial to be divided is fed sequentially into the shift register with the most significant coefficient first. The quotient polynomial appears at the output of the shift register as the input polynomial is being divided. After the input polynomial has been entered into the shift register, the remainder polynomial is left in the shift register stages. In the division mode, the shift register divides by $1 + x^3 + x^7$ for m - 7 and by $1 + x^2 + x^3 + x^4 + x^8$ for m = 8.

There are three design options for the programmable shift register/pattern generator including the direct form realization, and two forms of transpose realization. The direct form realization was chosen due to the minimum level of gate delays in the feedback connections. Figure 5.2-1 shows the logic diagram of the direct form realization of the programmable shift register/pattern generator. The seven and eight stage shift register/pattern generator in the AR6 mask set are designed as two individual circuits, and each contains two control lines to provide the four distinct modes of operation. The two pattern generators are configured in pairs on the same chip so that they can feed through a single EOR gate correlation output circuit to produce a gold-code of $(2^7 - 1)(2^8 - 1)$ bit long. They are also capable of operating independently in different modes.

Figure 5.2-2 shows the logic diagrams of a double clocked OR/NAND master slave flip-flop which is used to implement the register stages. It was chosen over a D-flip-flop type due to the speed performance requirement for 1-2 GHz clock frequency. The OR/NAND master slave flip flop has a maximum operating frequency of $1/2.3\ \tau_0$ while the NOR implemented D flip flop requires $1/5\ \tau_0$. SDFL NOR gates are used to implement the EOR logic between shift register stages. Figure 5.2-3 and Figure 5.2-4 show the equivalent logic diagrams of the seven and eight stage shift register/pattern generator, respectively.

Circuit simulations of the double clocked OR/NAND master slave flip flop revealed that its speed performance was critically sensitive to the duty cycle of the two clock inputs and the relative phase shift between CK



CONTROL 1	CONTROL 2	CONTROL 3	FUNCTIONS	COMMENTS
1	0	0	LOAD LENGTH 7 REGISTER	7 STAGE DELAY LANE
1	0	1	LOAD LENGTH 8 REGISTER	8 STAGE DELAY LANE
0	1	0	GENERATE PN SEQUENCE,	127 LENGTH
0	1	1	GENERATE PN SEQUENCE,	255 LENGTH
1	1	0	DIVIDE BY P7(X)	$P9(X) = 1 + X^3 + X^7$
1	1	1	DIVIDE BY P8(X)	$P8(X) = 1 + X^2 + X^3 + X^4 + X^7$
0	0	0	READ RESIDUE, LENGTH 7	RECIRCULATING MEMORY
0	0	1	READ RESIDUE, LENGTH 8	

Fig. 5.2-1 Direct realization of the programmable shift register/pattern generator.

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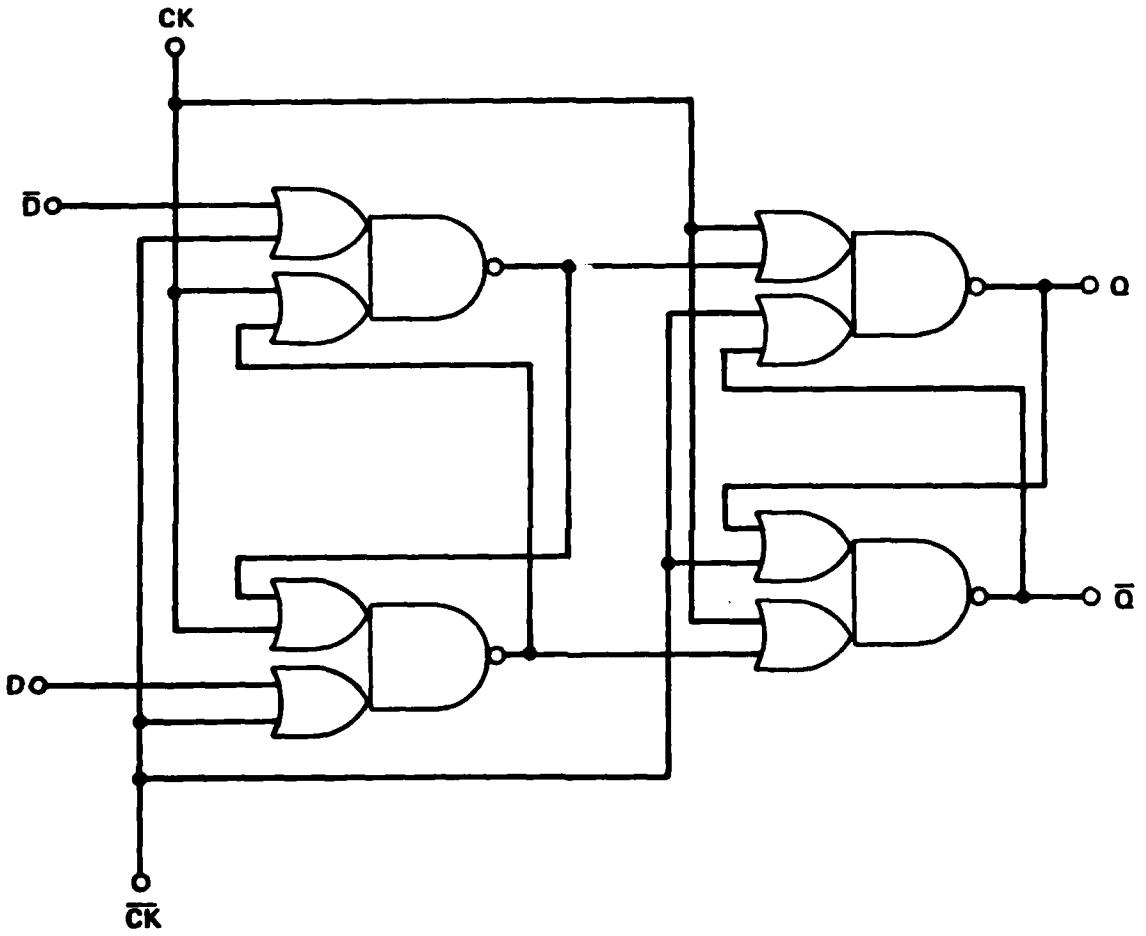

Fig. 5.2-2 Double-clocked OR/NAND master-slave flip-flop.

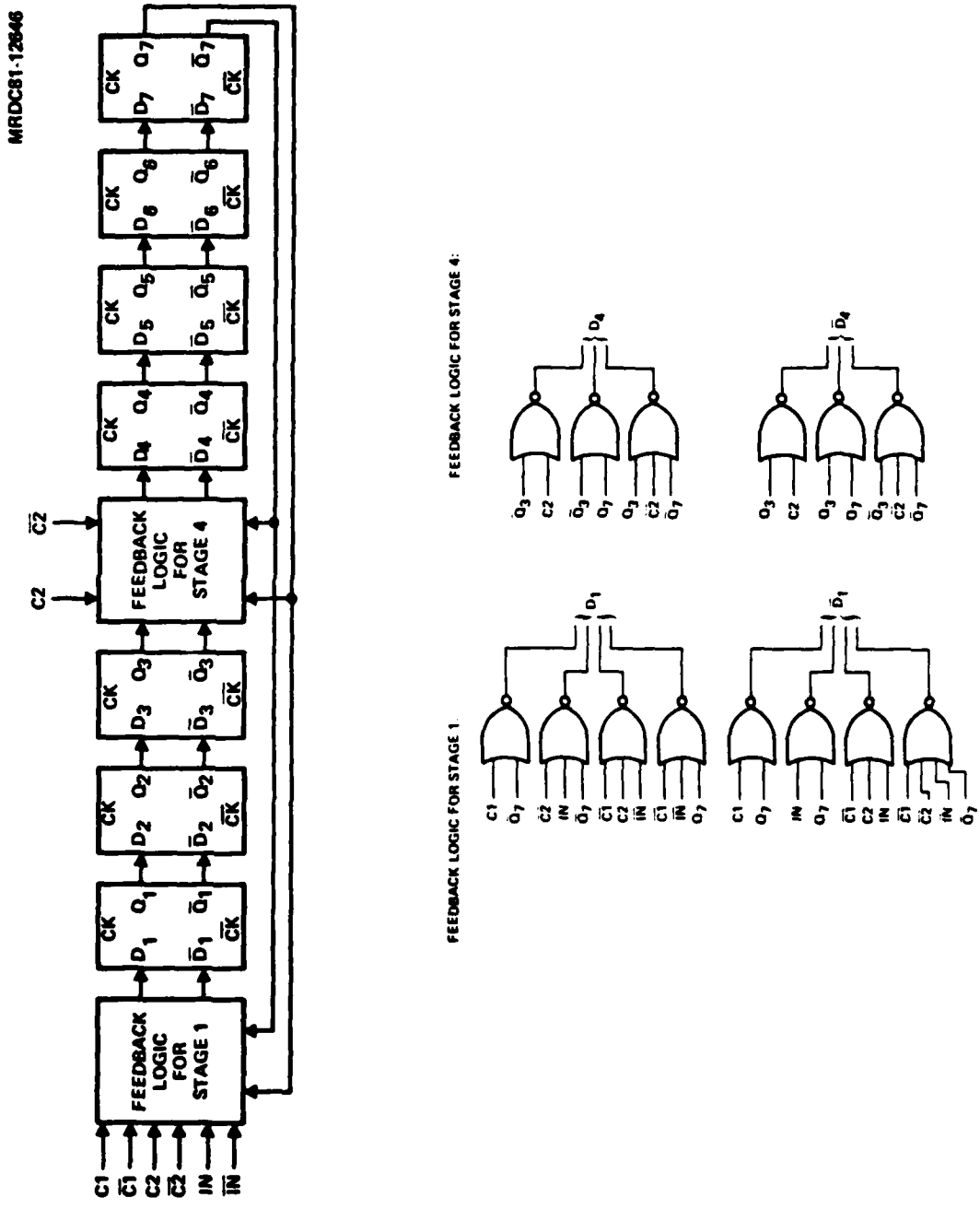

Fig. 5.2-3 Equivalent logic diagram of the 7-stage programmable shift register/pattern generator.

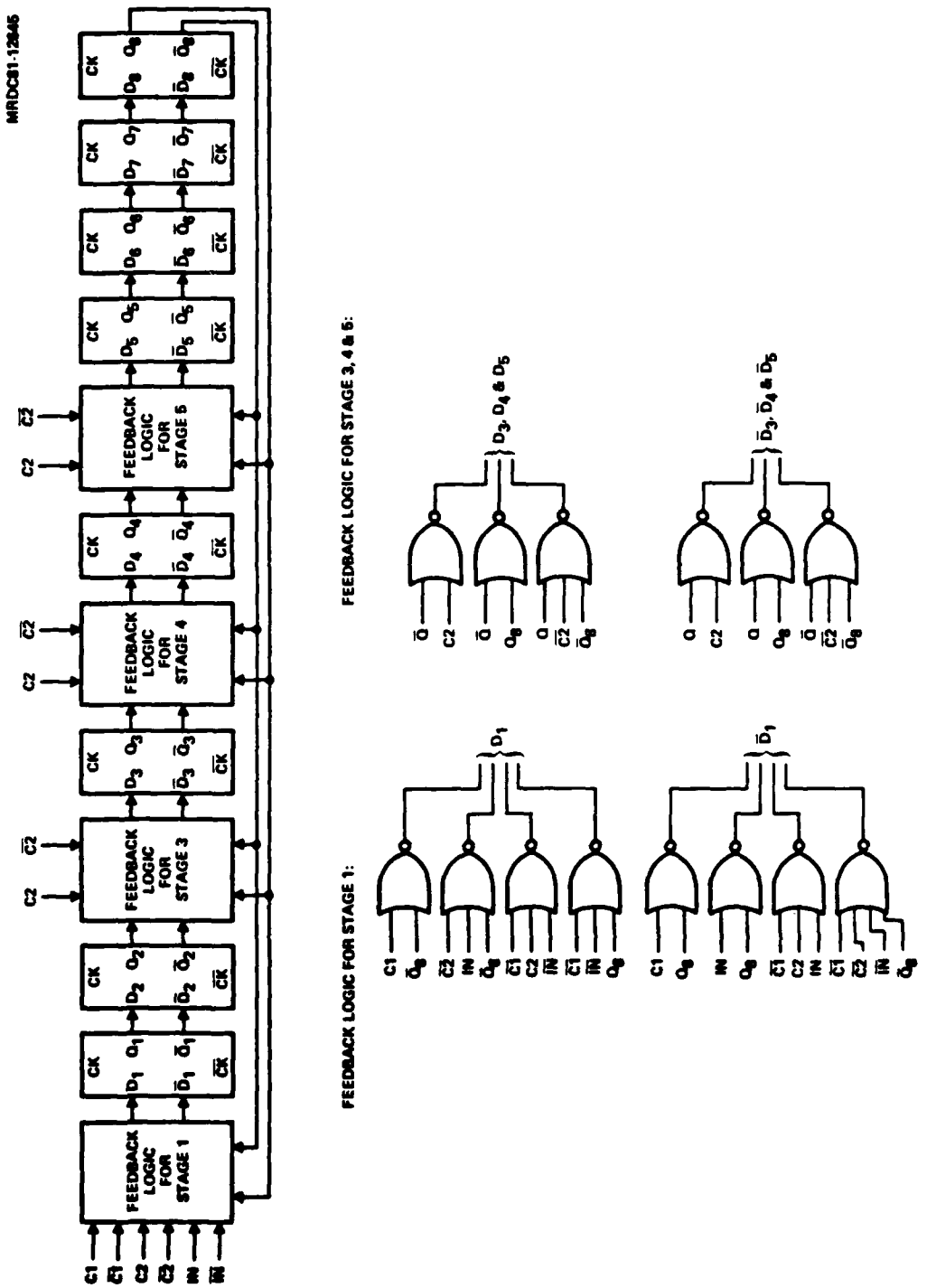

Fig. 5.2-4 Equivalent logic diagram of the 8-stage programmable shift register/pattern generator.

and $\overline{CK}$. This is understandable, since the gate propagation delay caused by signals propagating through the upper gate of the dual-gate switching FET in a OR/NAND gate is shorter than that through the lower gate. Also, the rising edge of the input waveform causes a faster transition of gate output than the falling edge in SDFL gates. To solve the problem, a flexible clock driver circuit was used to produce CK and $\overline{CK}$. Figure 5.2-5 shows its circuit diagram with two external controls V_{TH1} and V_{TH2} that independently adjust the duty cycles of CK and $\overline{CK}$. The use of separate pull-down supplies for each clock phased allows us to provide desirable relative phase shift between CK and $\overline{CK}$. To minimize the delay and relative phase shift of clock inputs between shift register stages, effort was made in the layout to equalize the length of clock signal lines feeding into all stages. The option of using direct CK and $\overline{CK}$ inputs was also provided.

The pattern generator circuits were incorporated on mask set AR6. Wafer fabrication was discussed in Section 4.4. A photograph of the circuit is shown on Fig. 5.2-6. When the circuits were tested, it was discovered that one of the pattern generators suffered from a layout error which caused one of the power supplies to be shorted. Testing was continued on the other circuit, without encouraging results. The circuit did not operate as a whole. Therefore, the clock section and the pattern generator section were examined separately, the latter by overriding the internal clocks with external ones. The limited testing done suggested that the circuit was suffering from some anomalies in the logic levels. Testing was not completed due to other priorities in the program. However, it was quite clear that a design iteration would be required before fruitful results could be obtained.

5.3 Feasibility Analysis of GaAs Mask Programmable Functions and Logic Arrays

The feasibility analysis portion of the program, funded by ERADCOM, was initiated as a four month definition and analysis phase of a multi-phase program, leading to the development of GaAs programmable kit parts and other high performance critical circuits applicable to future high speed communication systems operating in the frequency range > 1 GHz.

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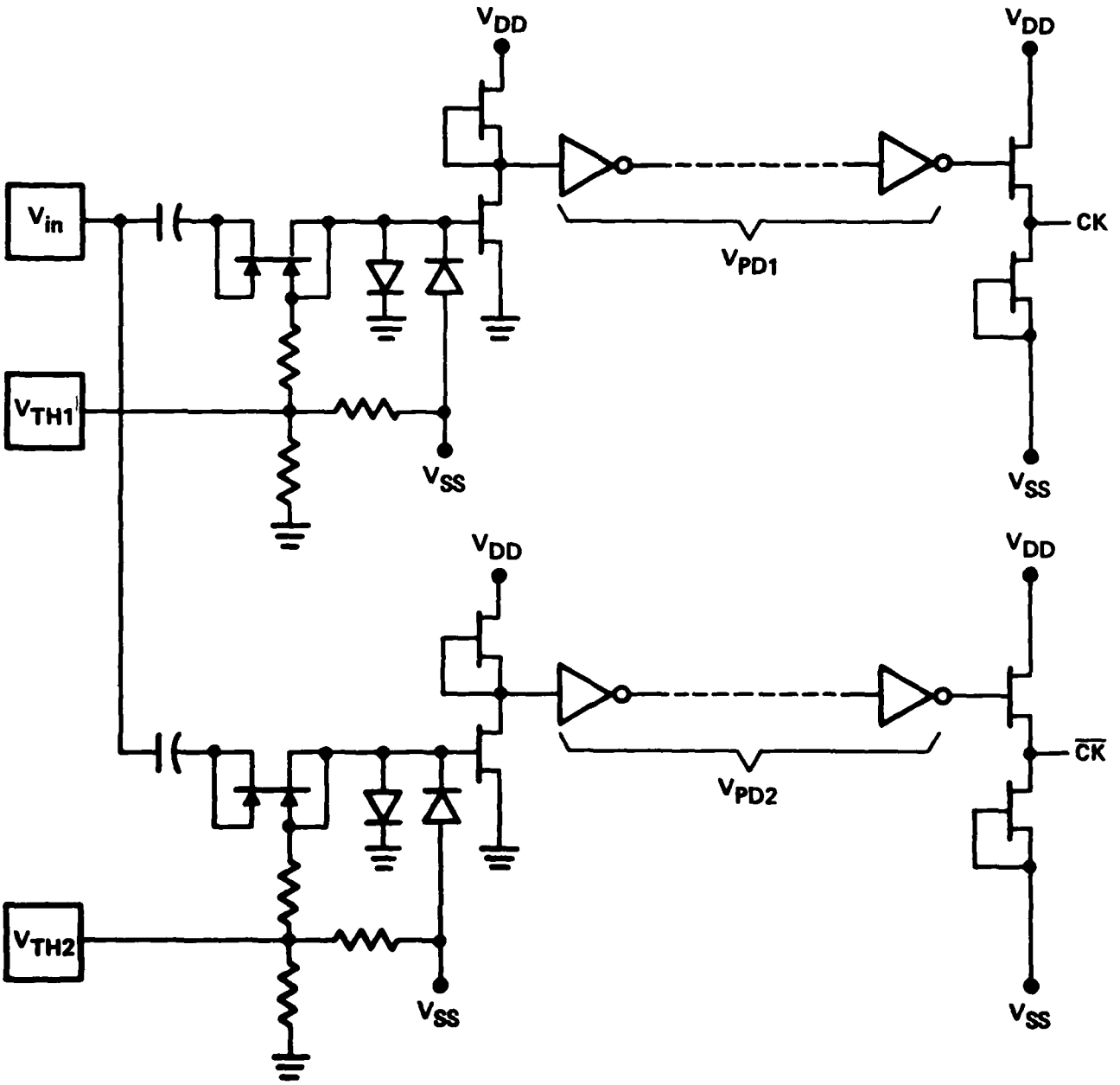

Fig. 5.2-5 Clock driver circuit for the programmable shift register/pattern generator.

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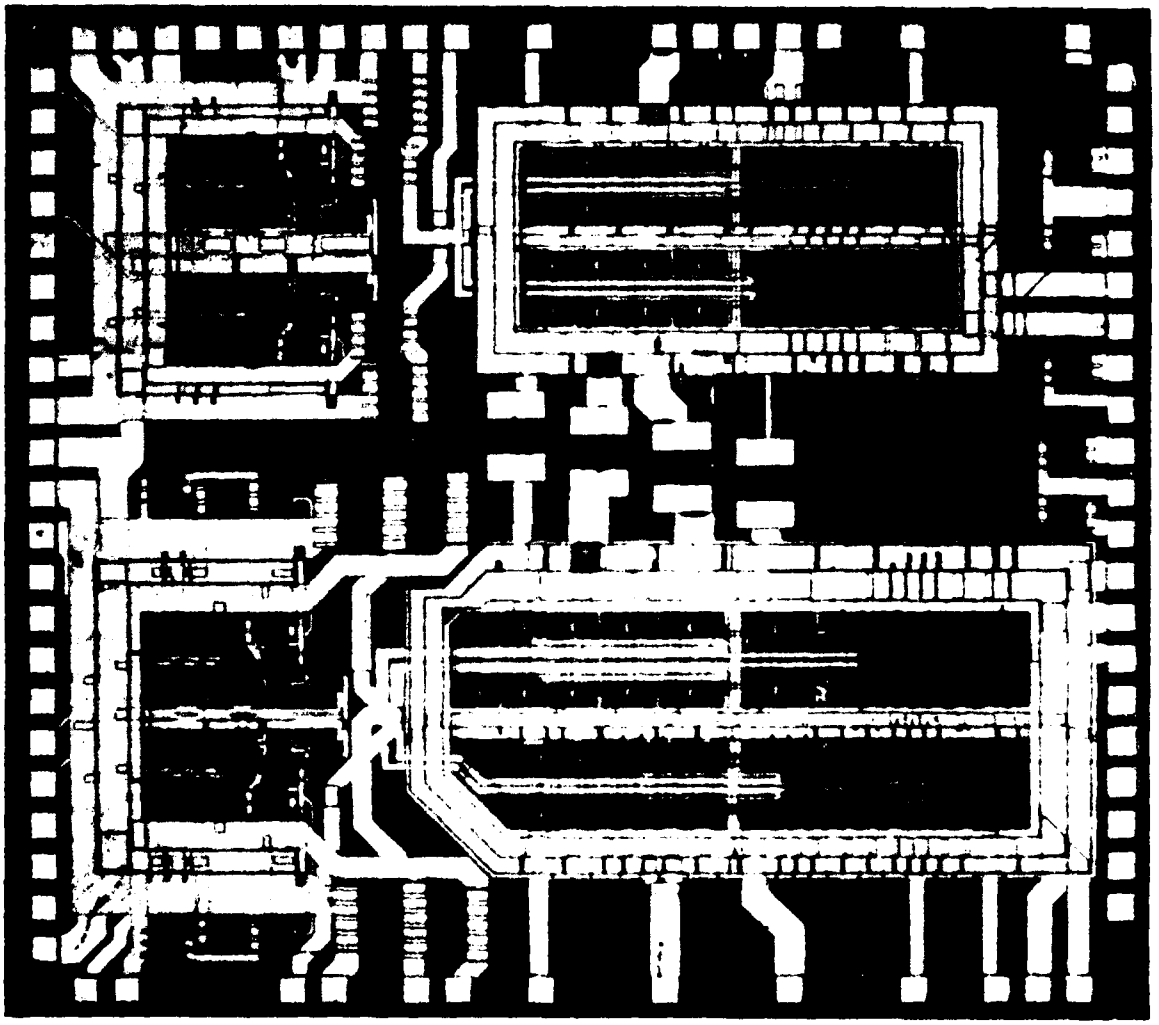

Fig. 5.2-6 Photograph of the 7-stage and 8-stage pattern generator chips.

A brief outline of the program and results follows. For complete details of the study phase, refer to Appendix A which is included as part of this final report.

During Phase I, a study of the various design approaches to GaAs was performed to determine which would be best suited to the particular application. For instance, Schottky diode-FET logic (SDFL), direct coupled logic using enhancement-mode MESFETs, buffered FET logic (BFL), and other circuit approaches were analyzed based on maximum speed, speed vs power and size vs speed/power. The conclusion from this analysis was that BFL was the most suitable candidate for implementing the various circuit functions.

A list of candidate circuits/functions which would be incorporated within the cells was developed through a coordinated effort between MRDC (Rockwell Microelectronics Research and Development Center (Anaheim, CA)) and CTPD (Rockwell/Collins Telecommunications Products Division (Cedar Rapids, IW)) personnel. Upon completion of the list, it was reviewed with ERADCOM to select the initial elements for the test chip.

The chip proposed will consist of six to nine cells ranging from 1.25 to 2 mm in size. These cells were selected in concurrence with the ERADCOM from the list below, as well as from new ideas which emerged during the study phase. Candidates for the cells included:

1. MSI Gate Array - Low cost design approaches require gate arrays in the range of 100 to 1000 gates, including I/O circuits.

2. Mask Programmable Prescalers - Required in high performance frequency synthesizers with divider ratios of 10/11, 20/21, 40/41 and 80/81.

3. Mask Programmable PN Sequence Generator - High speed PN sequence generators are used in systems where polynomial generation is required for data randomization and cyclic redundancy checks

(error correction); the proposed generator will have a maximum of (2n-1) bits when n = 20 flip-flop stages.

4. Linear Amplifiers and Voltage Comparators - High performance amplifiers and voltage comparators are applicable to high speed signal conditioners/buffers, AGC circuits, flash converters, D/A converters and alternate A/D converter approaches.

5. Phase Discriminator - Building block required as part of a complete phase loop (PLL) associated with frequency synthesizers.

6. Filters - Communication systems require filters for band limiting, passing and shaping. The filter could be composed of linear amplifiers and external components, or it could be designed using the switched capacitor approach.

7. Voltage Controlled Oscillator - VCOs comprise another building block required to complete a PLL. As an active element within the loop control voltage (DC), it is normally derived from the filtered output of a phase discriminator.

8. Four Bit Look Ahead Adder and Subtractor - Adders and subtractors are primarily used in signal processing and control systems requiring the four basic arithmetic functions of add, subtract, multiply and divide.

9. Four Bit Accumulator - Building block associated with the design of direct digital frequency synthesizers.

10. Shift Registers - Shift registers are applicable to signal processing, accumulators, correlation, multiplier/divider circuits and control systems.

From the suggested kit parts, as listed in the program outline, certain circuits were selected to be implemented in the first mask set to be produced during the following phase of the program. The circuits were prioritized as follows:

1. Interconnect and device modeling structures.
2. Process monitors.
3. Mask programmable prescalers - divide by 6/7, 10/11, 20/21 and 40/41.
4. Phase detector.
5. Binary down converter with synchronous load and asynchronous clear.
6. Pseudo random sequence generator - implemented in a storage/logic array and custom layout if time permits.

A third element of the analysis addressed the design and layout techniques required to achieve the high performance required of these critical elements. The applicability to GaAs of SYMCAD, an advanced symbolic design methodology developed for CMOS design, was evaluated. SYMCAD possesses several concepts such as interactive composing of circuit topology and an algorithmic mask generation which can be utilized, with proper symbol definition, to optimize layout of GaAs ICs for maximum performance.

Specific features of SYMCAD which were attractive for this GaAs design task were evaluated. These include:

1. Interactive composing of circuit topology, including concurrent design rull checking.
2. Algorithmic mask generation.

3. Single node circuit analysis based on actual circuit layout, including all parasitic elements and proximity effects.

The SYMCAD study indicated that the methodology used could be converted from CMOS/SOS to GaAs application with the introduction of new circuit elements and devices. Also, algorithmic and software extensions are required by GaAs technology because it uses more active elements and nonsymmetrical circuitry. A two year program schedule which would cover the complete conversion of SYMCAD from the CMOS/SOS to a GaAs environment is included in Appendix A.

6.0 RADIATION HARDNESS OF GaAs DIGITAL INTEGRATED CIRCUITS

GaAs integrated circuits offer high radiation tolerance, which makes them attractive for space applications. In this program two aspects of the radiation tolerance of GaAs IC's were evaluated. One is total dose effects, discussed in Section 6.1, and the other is transient ionizing radiation effects, discussed in Section 6.2. In general, it was found that the GaAs circuits are capable to receive total gamma doses on the order of 5×10^7 rads without experiencing any major change in their operating characteristics. The threshold for transient radiation upset was as high as 10^{10} rad/s if the circuit was properly biased. Transient radiation behavior was sensitive to circuit design and operating conditions.

6.1 Total Dose of Gamma Radiation

GaAs Schottky diode FET logic integrated circuits were evaluated for total dose sensitivity. Three stage ripple D flip-flop divider circuits (divide by 8) were selected for radiation testing because they are of MSI complexity (25 gates), they are easily evaluated, and most importantly, they represent real sequential logic circuits with typical fanouts of 2 to 3 in their D-FF latches. This latter condition is important to assure relevant test results, because noise margins and therefore logic upset levels are sensitive to fanout. Quite different results might be obtained on F.O. = 1 ring oscillator inverters, even on the same wafers.

The SDFL divide by 8 circuits were packaged in 16 pin flatpacks. Correct operation was observed at clock frequencies up to 1.35 GHz on these particular samples, at a total power dissipation of about 100 mW. An electrically shielded test fixture in which the circuit under test was powered by batteries to minimize possible pulse EMI problems was prepared. The divide-by 8 output was monitored remotely during the test. A 250 MHz signal was provided as a clock input.

Total dose measurements under active, biased device operation were made to verify that degradation of device performance would not be induced by irradiation of a functioning logic circuit. Previous total dose measurements had been carried out on unbiased devices with up to 50 MRad of Co^{60} gamma radiation exposure being applied without noticeable change in device performance. A Co^{60} source at the RADC Radiation Test Facility, Hanscom AFB, MA was used to carry out these tests.

No variation in device operation or functionality was observed during the total dose test. The only change observed was a gradual reduction in supply current (I_{SS}) from -13.1 mA before exposure to -11.8 mA after exposure to the 5×10^7 Rad total dose. This observed 10% reduction in supply current was probably a consequence of channel mobility degradation by lattice displacement caused by the radiation damage.[20] The slightly lower currents would be expected to reduce the maximum clock frequency by about the same percentage, a relatively minor effect from such a massive radiation dose. A summary of the measured peformance as a function of total dose is given in Table 6.1-1.

Table 6.1-1

Divide by 8 Circuit Operating Conditions While Accumulating a 5×10^7 Rad Total Dose
The only change observed was a 10% reduction in supply current.

V_{DD} = 3.46 V; V_{SS} = 2.2 V, V_{PD} = -2.99V; f_{clock} = 250 MHz.
The Co^{60} source dose rate was 2.75 MRad/hr.

Total Dose (Rad)	ISS (mA)
0	-13.09
1×10^7	-12.69
2×10^7	-12.12
3×10^7	-11.99
4×10^7	-11.92
5×10^7	-11.82

In order to evaluate the radiation tolerance of a complex circuit, a wafer containing a fully functional 8 × 8 bit parallel multiplier was exposed to a total dose of 5×10^7 rads. The circuit was retested after irradiation. The circuit had remained fully functional with minor shifts of its operating characteristics. For example, the biasing conditions required to obtain the maximum operating speeds were slightly changed (changes on the order of 0.1 V), but the actual maximum speed was not degraded.

6.2 Hardness to Transient Radiation

GaAs sequential logic circuits were evaluated under transient radiation. The circuits selected were ripple dividers built with D flip-flops, very similar to those used for the total dose experiments discussed in Section 6.1. Two versions of the circuits were tested. One employed standard MESFET active loads while the other employed saturated resistors as pull-ups in the SDFL gates.

A schematic of a standard SDFL NOR gate D flip flop is shown in Fig. 6.2-1. The NOR gates are combined to form D-type flip flops. Two such flip flops were cascaded to form a ripple type divide by four circuit, with a source follower capable of driving a 50 Ω load as is shown in Fig. 6.2-2. These circuits typically operate at maximum clock rates between 1.9 and 2.2 GHz at standard bias voltages (not optimized).

The saturated resistor used as a pullup in some of the circuits tested, is a gateless FET.[21] It has a nonlinear I-V characteristic which more closely resembles that of a transistor than that of a resistor, due to velocity saturation. The absence of the Schottky gate allows the saturated resistor to carry more current per unit width. It is therefore only 40% of the size of an equivalent transistor, and is less sensitive to backgating.[21]

A special control voltage was provided on the circuits used in this experiment, to adjust the pulldown current. This control voltage, V_{pd} in Fig. 6.2-1 is the gate bias voltage on the pulldown transistors. The V_{pd} is biased negative with respect to V_{SS}, the current flowing through the pull-downs is reduced. As a result, the fan-out capability of the NOR gate is increased, at

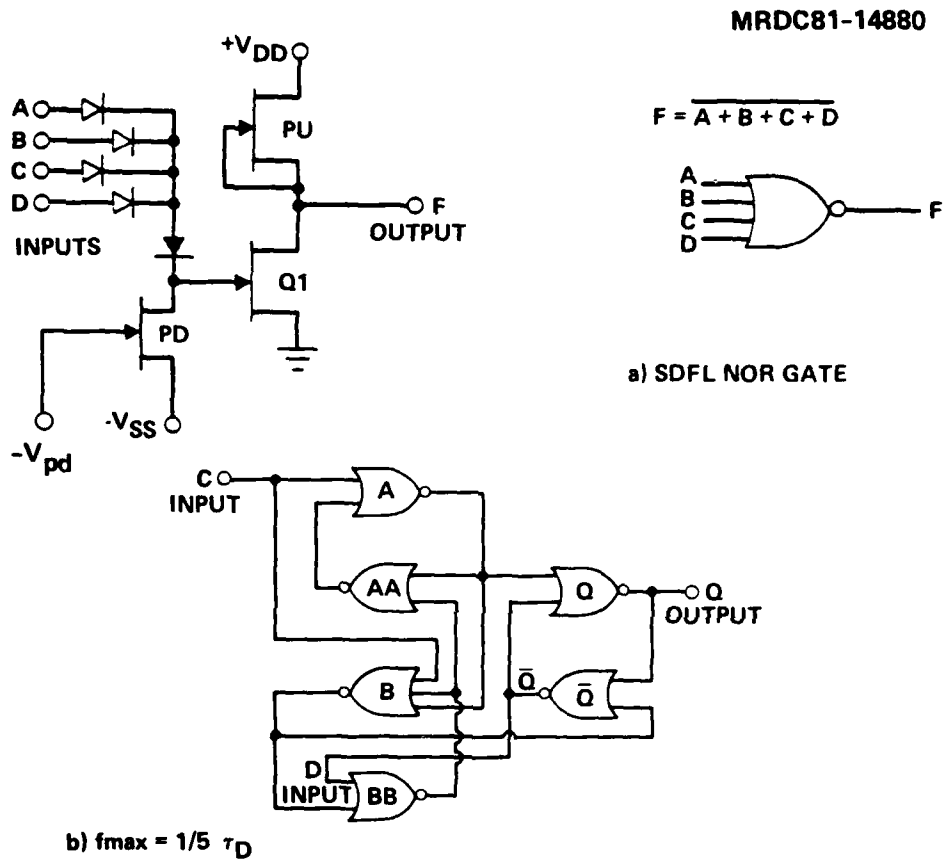

Fig. 6.2-1 a) Schematic and logic diagram of a SDFL NOR gate. b) Logic diagram of a D type flip-flop built with NOR gates.

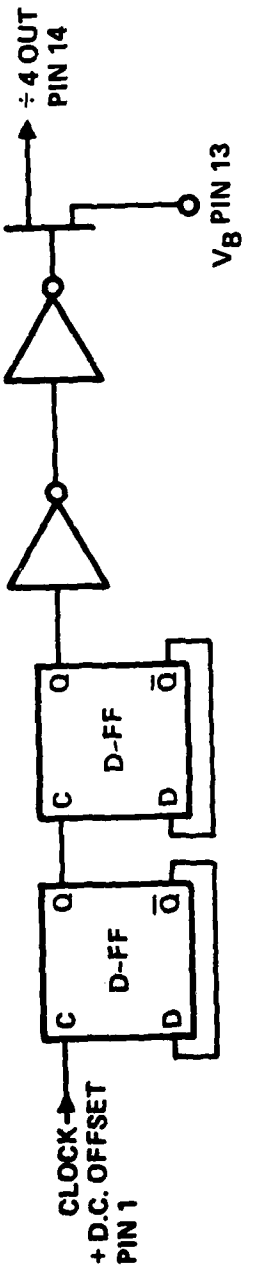

Fig. 6.2-2 Logic diagram of a ripple type divide by four circuit formed by two cascaded D type flip-flops with a source follower output driver.

the expense of speed, because the lower pulldown current implies a slower discharge of the switching FET's gate, when it goes from "on" to "off."

The experiments were performed at two locations; the Naval Research Laboratory (NRL) in Washington, D.C., and the White Sands Missile Range in New Mexico. A linear accelerator (LINAC), provided the electron beam used to irradiate the circuits. The duration of the radiation pulses ranged between 20 ns and 60 ns. The dose rate was determined by the distance between the radiation source and the device. Dose rates ranged between 1×10^8 and 2×10^{10} rads/s. Measurement of the radiation dose of each pulse was made using either a thermoluminescent device (TLD) or a silicon PIN diode.

The main effect that the radiation pulses had on the devices was to increase the positive supply current, I_{dd}, and to change the output level. Both returned, following an exponential envelope, to the levels preceding the pulse. The time required to return to within 10% of the initial value will henceforth be referred to as the decay time. This is to be distinguished from the recovery time, which is the time required for the circuit to resume proper operation following an upset.

The long term transients were observed with a storage oscilloscope. This allowed for the convenient evaluation of the decay times, which in some instances were as long as 1 s. The output signal, in the immediate vicinity of the radiation pulse, could not be clearly seen with this method. The short term disturbances were observed using transient digitizers, where the output signal could be clearly seen in the immediate vicinity of the radiation pulse, but the sampling memory of the digitizers were insufficient for viewing longer envelopes. Therefore, the data from the two experiments complemented each other quite well. Samples of extended, and short time scale data are shown in Figs. 6.2-3 and 6.2-4, respectively.

Figure 6.2-3 shows long term effects in a divide by four circuit, as it is exposed to a pulse of 2×10^{10} rads/s. The upper oscillogram was taken with the positive bias voltage $V_{dd} = 2.5$ V, and the lower oscillogram was taken with $V_{dd} = 3.0$ V. There are two traces on each oscillogram. The upper trace depicts the divide by four output, and the lower trace depicts the

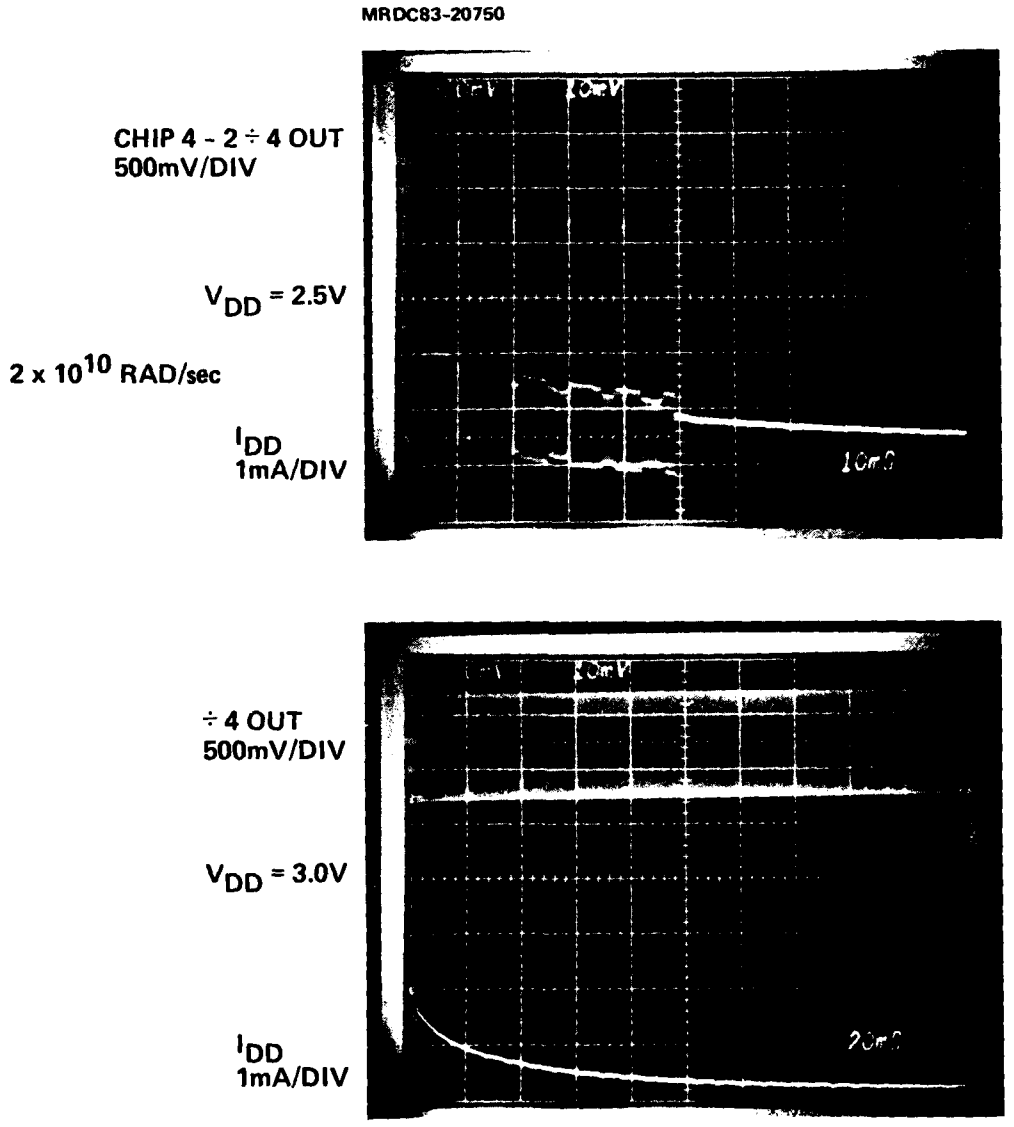

Fig. 6.2-3 Oscillograms showing long-term transients in a divide by four circuit. The radiation dose rate was 2 x 10^{10} rad/s. The two traces in each oscillogram correspond to the output signal and the positive supply current, I_{dd}, respectively. The top figure corresponds to V_{dd} = 2.5 V, and the bottom figure to V_{dd} = 3.0 V. The duration of the hash in the upper oscillogram corresponds to the recovery time.

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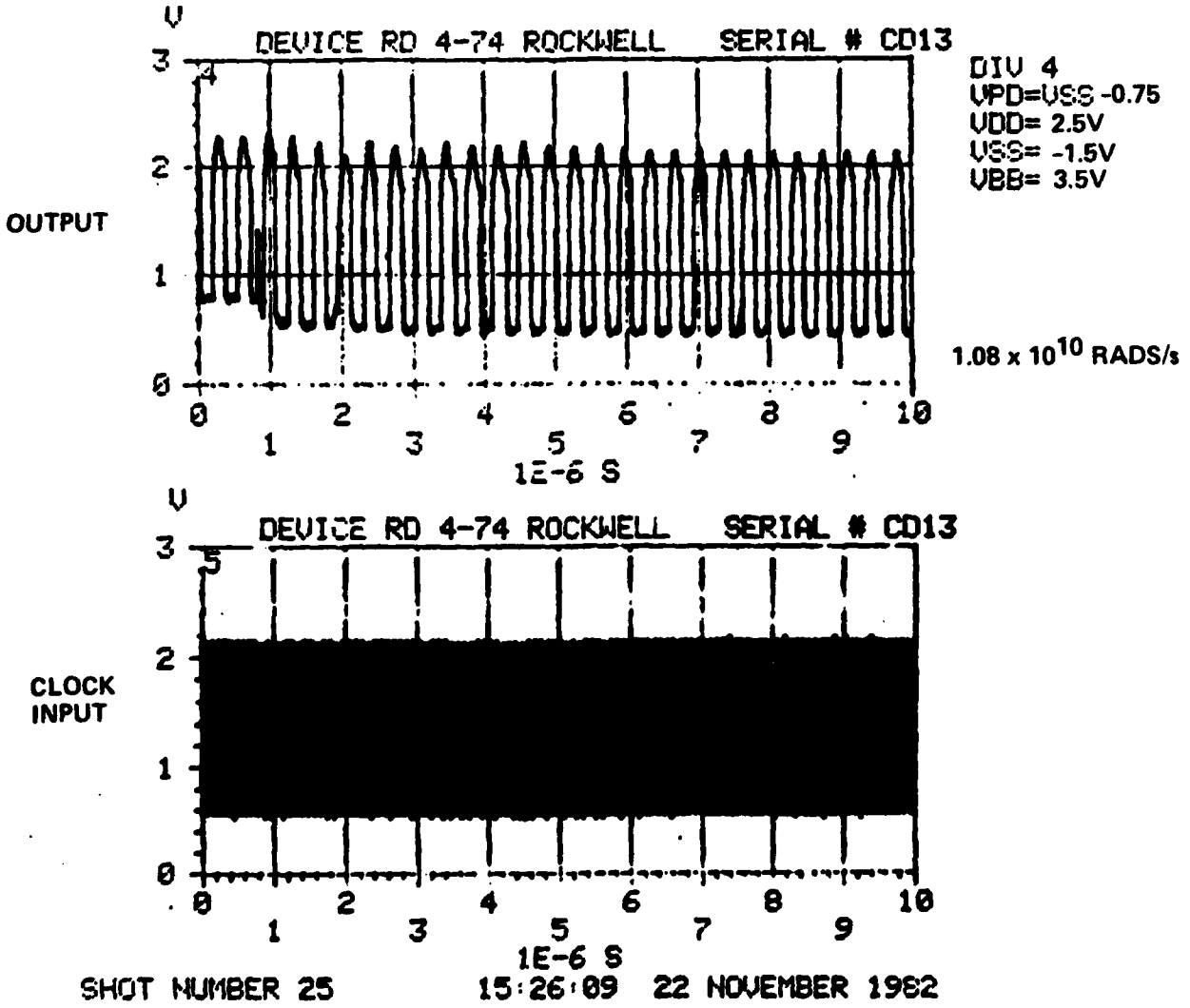

Fig. 6.2-4 Divide by four output (top) and clock input (bottom) in the immediate vicinity of a 1.08×10^{10} rads/s radiation pulse. The control voltage V_{pd} was adjusted to V_{ss} = 0.75 V. The circuit performs the divide by four operation without being interrupted by the radiation pulse.

positive supply current, I_{dd}. Figure 6.2-4 shows a short term effect in another divide by four circuit, as it was exposed to a pulse of 1×10^{10} rads/s. The upper waveform is the divide by four output, and the lower waveform is the clock input.

The observed devices showed various degrees of perturbations over the range of dose rates evaluated. The consistent trends that were observed are as follows: there is an expected increase in the amplitude of the positive supply current, I_{dd}, and the decay time increases as the dose rate increases. Increasing the positive supply voltage, V_{dd}, decreases the decay time. This is exemplified in Fig. 6.2-3. Although it is difficult to see exactly what is happening to the output waveforms from the oscillograms, it can be easily inferred that during the period where there is hash on the corresponding current waveform, such as in the upper oscillogram of Fig. 6.2-3, and the circuit is not dividing correctly. The hash represents changes in the supply current corresponding to state changes of the counter. When the circuit divides correctly, this hash is not seen because the frequency of the current changes is higher than the bandwidth of the amplifier used to monitor the current. Therefore the hash indicates that the circuit is changing states less frequently than that which is required for proper divide by four operation. The duration of the hash then, is a reasonable representation of the recovery time.

The 55 ms disturbance of the ÷4 output seen in the upper oscillogram of Fig. 6.2-3 is reduced to a 1 ms period (barely detectable in the lower oscillogram) when V_{dd} is increased. Other oscillograms taken under the same experimental conditions, with shorter time sweeps, indicate that for most of the 1 ms period, the output is dividing correctly, and the major disturbance is a small shift in the output level that does not affect circuit functionality. Another indication that the recovery time is extremely short in the lower oscillogram is the fact that no hash is detectable on the corresponding current waveform. The time required for the circuit to resume the divide by four operation is far shorter than the decay time.

As V_{pd} is adjusted, and made increasingly more negative with respect to V_{ss}, the time for which the circuit is not dividing correctly is reduced to the point where divide by four operation is not affected even at dose rates as high as 1×10^{10} rads/s, as shown in Fig. 6.2-4. Here, V_{pd} was biased 0.75 V below V_{ss}. Under the same radiation conditions, with V_{pd} 0.3 V beneath V_{ss} the same device would sometimes miss a count, and not resume proper operation until 3.5 μs after the radiation pulse. With V_{pd} 0.15 V beneath V_{ss}, this device did not divide properly for more than 10 μs after the radiation pulse. Thus we see that V_{pd} can be used to improve transient radiation hardness. However, this is accomplished at the expense of maximum speed of operation. This tradeoff was unnoticeable at the low frequencies (< 250 MHz) used for these tests. Figure 6.2-5 shows data taken in a nonradiation environment, showing how the maximum operating frequency of the devices decreases as V_{pd} is biased negative with respect to V_{ss}.

Circuits designed using saturated resistor pull-ups were observed to be affected less than circuits with FET pullups. In several instances, circuits with FET loads would experience long term upsets, as shown in Fig. 6.2-3, where the divide by four output would not be correct, and I_{dd} would behave erratically. A similar circuit with saturated resistor loads would experience only a change in output level, and the I_{dd} decay time would be shorter under the same test conditions.

The results observed are consistent with those obtained in earlier experiments.[22] They indicate that pulsed ionizing radiation causes charge trapping in the semi-insulating GaAs substrate.[23,24] The higher the ionizing radiation dose, the more charge trapping occurs. The result is an effect very similar to that of backgating.[23]

The channels of the devices operating at the more positive potential (the pullups) appear to be the most severely affected. Therefore, when V_{dd} is increased, thereby increasing the current that the pullup devices can supply, the circuits are less disturbed by transient radiation.

Since SDFL circuits have a wide voltage noise margin, the circuits can still operate properly while the pull-up currents are altered. This

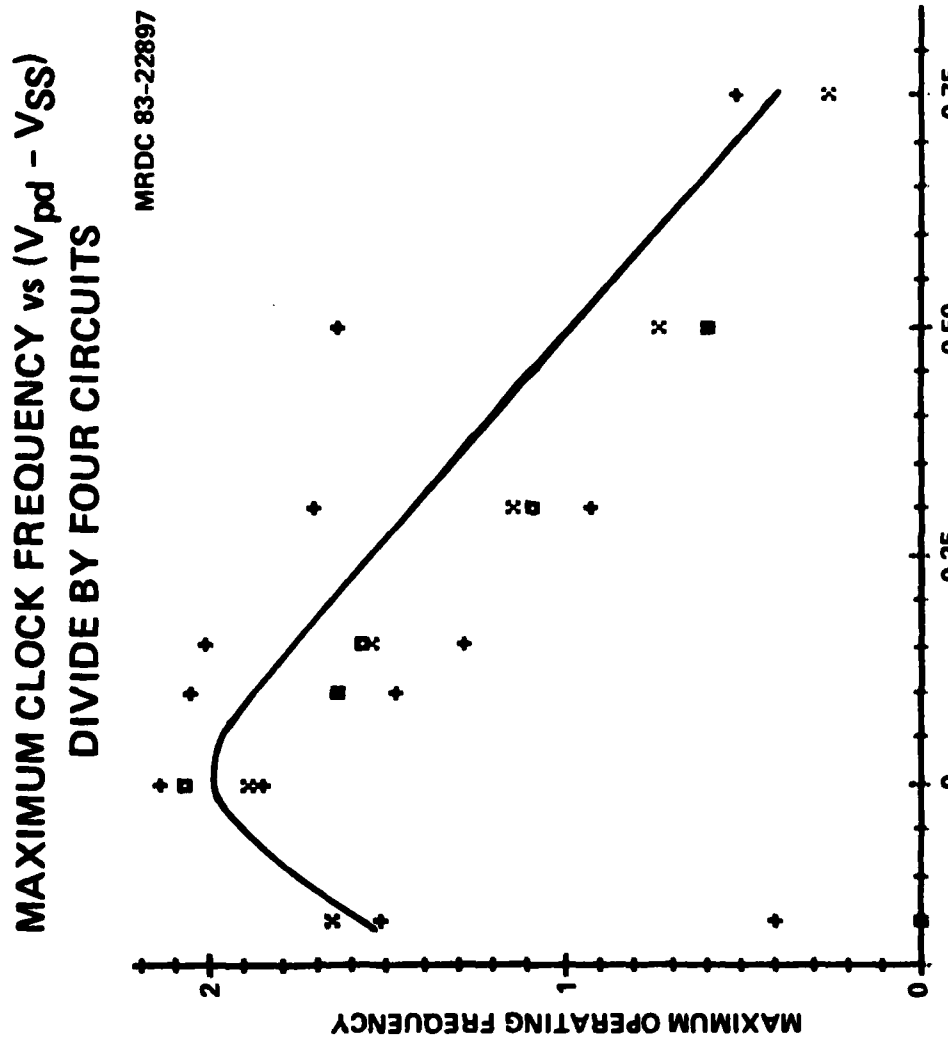

Fig. 6.2-5 Maximum input clock frequency vs (V_{pd} - V_{ss}) for divide by four circuits.

explains why the time required to resume proper logic operation (divide by four) is observed to be much shorter than the decay time. On the other hand, SDFL gates are sensitive to fanout because each gate is sinking current from the previous stage. If the ratio between pull-up and pull-down currents is reduced by radiation induced backgating, the circuit may fail to operate for the time when the pullup can not provide enough current to the following stages. Making V_{pd} more negative with respect to V_{ss} raises the upset threshold, and reduces the amount of pulldown current required (see Fig. 6.2-1). This reduces the burden on the pullups, allowing them to supply sufficient current to ensure proper logic levels. Note that the same effect obtained by adjusting V_{pd} can be achieved by designing shorter width pulldown transistors. Therefore, the additional control voltage, which is very convenient for experimental purposes, does not need to be provided when a radiation hard circuit is designed.

The saturated resistors were observed to be less affected by radiation than were the equivalent FETs. This can be explained by the fact that the saturated resistors channel is not initially depleted by the presence of a Schottky gate. Therefore a smaller fraction of the channel depth is depleted due to the charge trapped beneath the channel of the saturated resistor.

The experiments reported here confirm previous repors on the high tolerance to transient radiation of GaAs integrated circuits. These, along with high total dose hardness, are important assets for space applications of this technology. From these experiments, a variety of bias voltage adjustments, and design variations that can be used to control the divide by four prescalers upset thresholds over dose rates ranging from 1×10^8 to 2×10^{10} rads/s were determined. It was also shown how tradeoffs between speed and/or power dissipation can be made to increase transient radiation hardness, over a range of two orders of magnitude.

7.0 MODELING OF MESFET DEVICES

The major thrust of this activity which was carried out at North Carolina State University, was to develop accurate computer models for analyzing the performance of short-channel GaAs MESFET devices as used in the Rockwell VLSI circuits.

The modeling research was divided into three parts:

1. Two-dimensional finite difference simulation.
2. Two-dimensional Monte Carlo analysis.
3. Analytical modeling.

The intent was to use the two-dimensional analyses to give exact solutions to the device operation and to serve as a guide for developing a simpler, and less expensive, analytical model of sufficient accuracy to be valuable as a design aid and to study effects of parameter changes.

In addition, work has been carried out in the characterization of material and device properties using C-V and DLTS techniques.

In general, significant results have been obtained in all phases of the program. The work on the two-dimensional model led to good predictions of the major features of the ion implanted, 1 μm gate MESFET. The Monte Carlo analysis in general predicted currents almost three times higher than those obtained from a conventional 2D device analysis program. This result suggest that such conventional programs are inadequate for modelling of very small devices due to their lack of consideration of velocity overshoot and other transient phenomena. An analytical model based on a two-piece approximation of the velocity-field characteristics was proposed. This approximation is defined from a theoretical velocity-field characteristic obtained by Monte Carlo techniques. Finally, a measurement technique for determining free-carrier, shallow-level donor, trap and mobility profiles of ion-implanted devices has been successfully applied to a 1 μm gate length MESFET.

A detailed description of the work here summarized can be found in Appendix B of this report.

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